

OM

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VLSI

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① JFET:

→ Book: Microelectronics CKts by Sedra & Smith (old edition).

- Construction and operation of JFET.
- Drain Char. & Transfer Characteristics.
- JFET biasing.
- Amplifiers Analysis.
- Frequency Analysis.

Book

Boxle std.

② MOSFET:

→ Book: → CMOS VLSI Design by Weste & Harris (Ch-1, 2 & 4).

→ Design of Analog CMOS IC by RAZAVI (Ch: 2 & 3)

→ Depletion & Enhancement MOSFET.

→ Construction & operation of MOSFET.

→ Drain Char. & Transfer Characteristics.

→ MOS Capacitor. ④ ↴

→ MOSFET Analysis.

→ Amplifiers Analysis.

→ Frequency Analysis. ④ ↴

③ CMOS:

- Implementation of functions in CMOS Technology.

- Transfer char. of an inverter. ✓
- Transistor sizing.
- Rise time, fall time, propagation delay & contamination delay.
- Delay calculation.
- Power
- Noise margin.

④ Device Technology:

- IC fabrication technology:

Steps:

- ① Oxidation.
- ② Diffusion.
- ③ Ion-implantation.
- ④ Photolithography.

- n-tube (or) n-well.

- p-tube (or) p-well.

- Twin-tube (or) Double-well cmos process.

2)

Energy Band in Si (silicon):

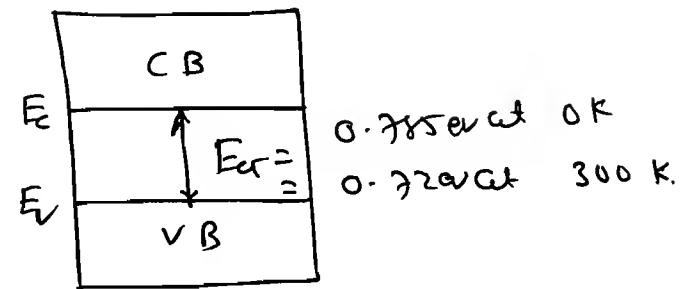
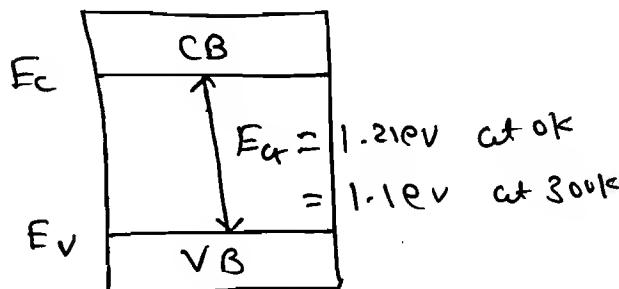
IMP

Concept: Why silicon (Si)?

Ans: • Low leakage current.

$$\left. \begin{array}{l} I_o(\text{Si}) : 2\text{A} \\ I_o(\text{Ge}) : 4\text{A} \end{array} \right\} I_o(\text{Ge}) \approx 1000 I_o(\text{Si}).$$

• More energy gap.



Si

Ge

→ Carrier concentration remain same for applied electric energy, it change only when thermal energy is applied.

• More Resistivity.

$$\rho_{\text{Si (Ge)}} = 44.6 \approx 45 \text{ } \Omega\text{-cm}$$

$$\rho_{\text{Si (Si)}} = 231.5 \text{ K} \approx 230 \text{ } \Omega\text{-cm.}$$

$$\rho_{\text{Si}} = \frac{1}{n_i(\mu_p + \mu_n)^2}$$

Si:

$$\mu_n = \frac{\text{millman}}{1300} \text{ cm}^2/\text{V-s}$$

$$\mu_p = \frac{500}{500} \text{ cm}^2/\text{V-s}$$

$$n_i = 1.5 \times 10^{10} \text{ /cm}^3$$

$$\mu_n = 1350 \text{ cm}^2/\text{V-s.}$$

$$\mu_p = 480 \text{ cm}^2/\text{V-s.}$$

Cre: Miltman

$$l_n = \frac{3800}{3} \text{ cm}^2/\text{V-s}$$

$$l_p = 1800 \text{ cm}^2/\text{V-s}$$

SMJ

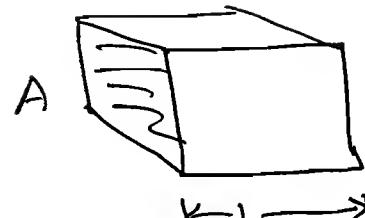
$$l_n = 3900 \text{ cm}^2/\text{V-s}$$

$$l_p = 1900 \text{ cm}^2/\text{V-s}$$

- More Resistance:

$$R_{(si)} = \frac{\rho_{(si)} L}{A}$$

$$R_{(core)} = \frac{\rho_{(core)} L}{A}$$



$A \& L$ same for the both.

$$R_{(si)} > R_{(core)}$$

So, more electron attenuation in si. So
Low leakage current in si.

• High Temp. (withstand).

$$Si \rightarrow 1425^\circ C$$

$$Cre \rightarrow 935^\circ C$$

• High Voltage (sustained).

→ VLSI stands for very large scale integration.

→ This is a field which involves integration (or) packing more & more devices in a smaller and smaller area.

⇒ All RF devices are made up of

Gallium Arsenide (GaAs)

GeAs: $\mu_n = 8500 \text{ cm}^2/\text{Vs}$.

$\mu_p = 400 \text{ cm}^2/\text{Vs}$.

→ Ge has high mobility for high current & high freq.

→ Si for low & medium freq.

→ npn is used instead of pnp because high mobility of electron in npn compared to pnp.

→ Bardeen, Brattain & Shockley was invented first transistor in 1948.

→ Shockley invented FET in 1952.

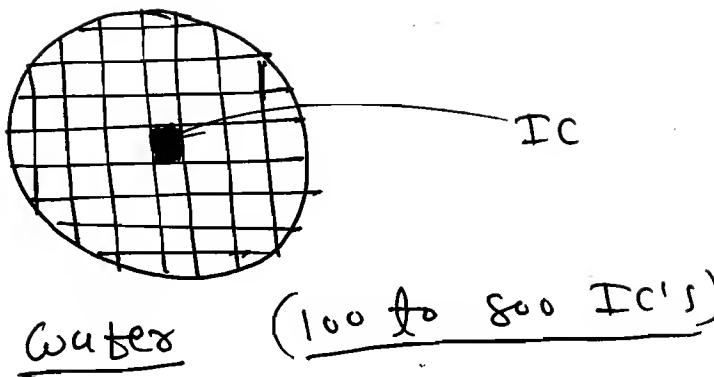
→ Jack Kilby invented IC in 1958.

→ Kotting & Attley invented MOSFET in 1960.

→ Integrated circuit consist of active & passive devices & also interconnection in a integrated (or) package on a single crystal of a Si chip.

→ IC fabrication is a wafer batch process that is more no. of CKTS & IC's can be fabricated at one go.

⇒



* Advantages of IC:

- Smaller size.
- Cost → Low
- Low Power
- High Speed
- Reliable
- Better performance.
- minimization & hence increase the equipment density.
- Cost reduction due to batch processing.
- Increase Reliability due to elimination of Soldering joints.
- Improved function of performance i.e. Complex circuitry can be fabricated with better characteristics.
- Increase operating speeds due to reduction of parasitics.
- Reduction in power consumption.

→ In 1965 Gordon Moore (founder of Intel) observed that transistor count becomes doubles for every 18 to 24 months. ⁴⁾

$$\rightarrow \frac{\text{Size}}{2} \Rightarrow \frac{\text{Area}}{2} = \frac{W \times L}{N^2 \sqrt{2}}$$

1	2	3	4	5
6	7	8	9	10

Scaling factor

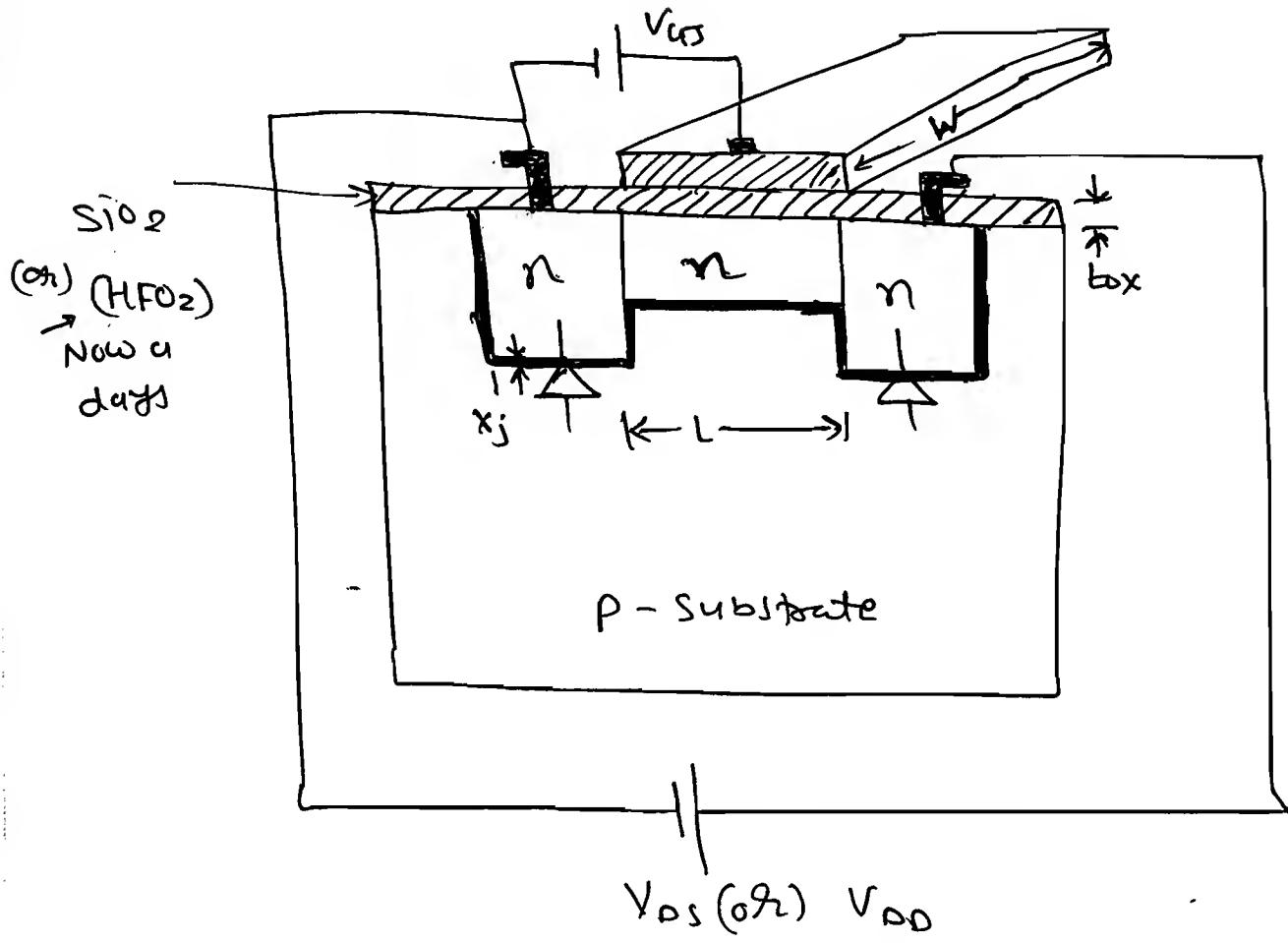
$$(s \text{ or } \alpha) = \sqrt{2}$$

<u>* Technology</u>	<u>Scaling</u> :- (in terms of <u>channel length</u>): L
L = 10 μm (400 GfP) (1971)	10 μm 6 μm 3 μm 1.5 μm 1 μm 0.8 μm 0.6 μm 0.35 μm 0.25 μm
	180 nm 130 nm 90 nm 65 nm 45 nm 32 nm 22 nm 14 nm
	now a day's.

→ Channel length (\uparrow) = Leakage Current (\uparrow) (power) (\downarrow).

* Scaling:

- ① Constant field scaling.
- ② Constant voltage scaling.



→ L = Channel length.

→ W = Channel width.

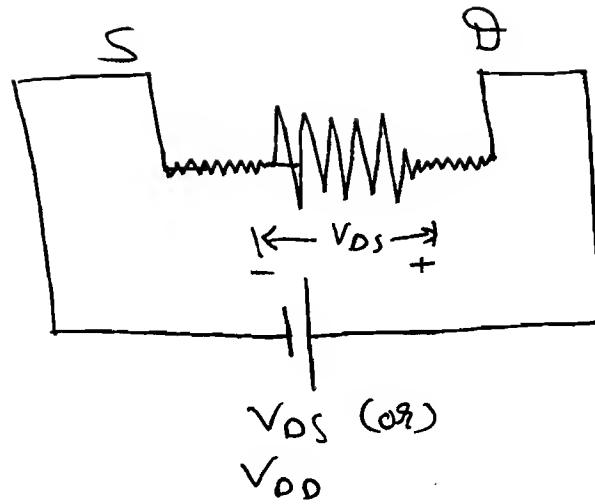
→ t_{ox} = Gate oxide thickness.

→ x_j = j^n depletion thickness.

→ V_T = Threshold voltage.

→ V_{DD} = power supply voltage.

→ $N_A (or) N_D$ = Substrate Doping concentration. (or) density.



$$E = \frac{V_{DS}}{L}$$

5)

① Constant Field Scaling:

⇒ Parameters

Before
Scaling

After
Scaling

① Channel length	L	$L' = L/s$
② Channel width	w	$w' = w/s$
③ Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/s$
④ Junction depletion thickness	x_j	$x_j' = x_j/s$
⑤ Threshold voltage	V_T	$V_T' = V_T/s$
⑥ Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/s$
⑦ Substrate doping density	N_A (or) N_D	$\frac{N_A'}{N_A} = S N_A$ $\frac{N_D'}{N_D} = S N_D$

$$W \propto \sqrt{\left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$$

②	Constant Parameter	Voltage	Scaling:	After Scaling.
			Before Scaling	
①	Channel length		L	$L' = L/s$
②	Channel width		W	$W' = W/s$
③	Gate oxide thickness		t_{ox}	$t_{ox}' = t_{ox}/s$
④	junction depletion thickness		x_j	$x_j' = x_j/s$
⑤	Threshold Voltage		V_T	V_T
⑥	Supply Voltage		V_{DD}	V_{DD} remain unchanged
⑦	Substrate doping density		N_A (or) N_D	$N_A' = s^2 N_A$ $N_D' = s^2 N_D$

* Level's of Integration:

① SSI: Such as 7404 has upto 70 gates per chip.
ex: logic gates, flip-flop.

② MSI: Such as 7416 counters have upto 1000 gates per chip.
ex: Counter ICs, multiplexers, Address.

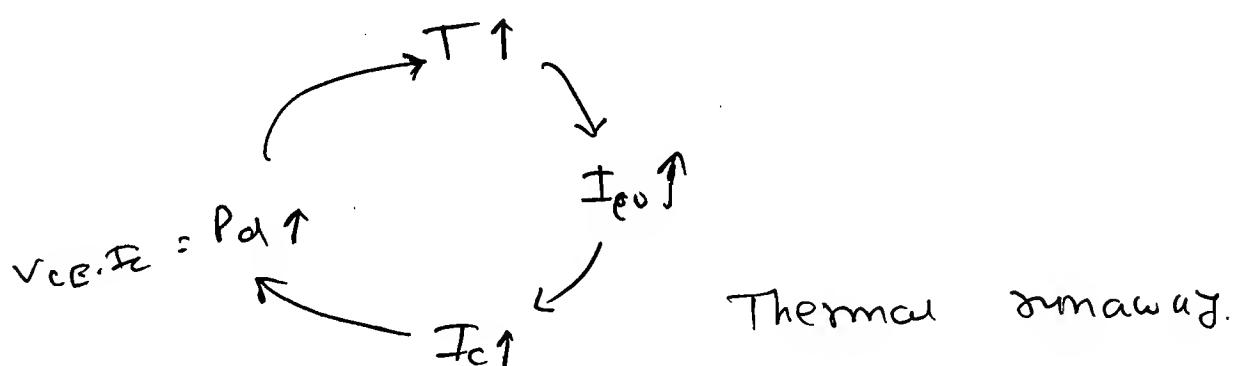
③ LSI: Such as simple 8-bit up have upto 10,000 gates per chip.
Ex: 8-bit up, ROM, RAM.

④ VLSI: More than 10,000 gates / chip.
(OR)
1 million Transistor / chip.
Ex: 16-bit up, 32-bit up.

1 - FET (Field Effect Transistor)

=> Advantages of FET.

- Unipolar
- Low cost
- Low noise
- Low Power
- Immune to radiation.
- High input impedance (use in CRO, voltmeter).
- Low offset voltage.
- Low thermal sensitivity.



=> Thermal Stability :

$$\frac{\partial P_d}{\partial T_j} < \frac{\partial P_o}{\partial T_j}$$

$$\Rightarrow V_{CE} < \frac{V_{CC}}{2}.$$

→ BJT → CCCS

$$T_p \uparrow \rightarrow I_o \uparrow \rightarrow I_e \uparrow$$

Positive temperature coefficient.

→ FET → VCCS

$$T \uparrow \rightarrow I_o \downarrow \quad P_o = V_{DS} \cdot I_o.$$

Negative temp. coefficient.

* Features of FET:

- ① Unipolar device because current is due to only majority carrier only.
- ② High input impedance.
- ③ Immune to Radiation.
- ④ Less noisy than BJT.
- ⑤ No offset Voltage at zero drain current.
- ⑥ Thermally more stable than BJT.
- ⑦ Simple biasing.

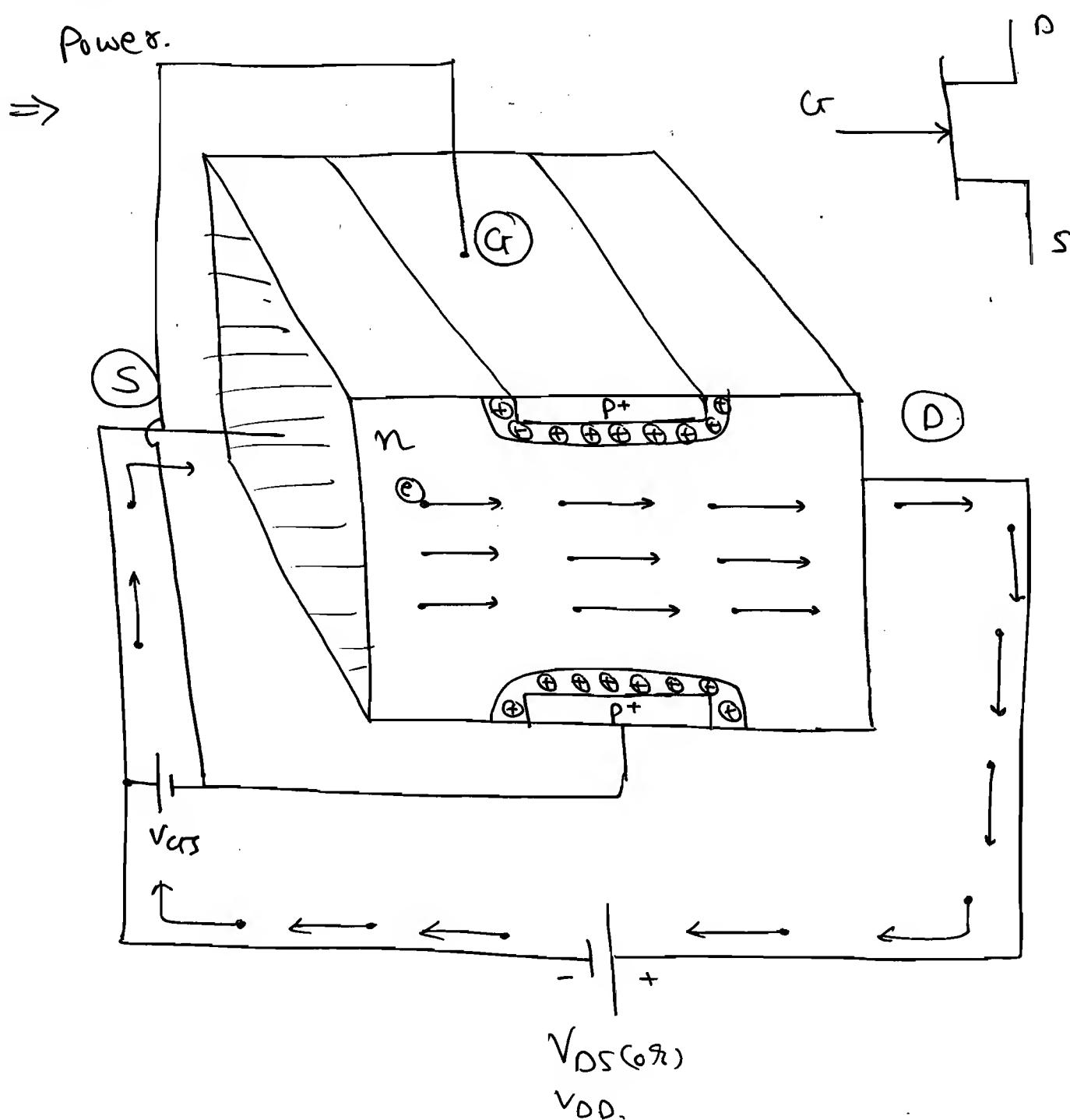
→ It requires less no. of fabrication steps therefore low cost.

→ Voltage Controlled devices that is VCCS.

* Drawback:

→ Low gain Bandwidth Product.

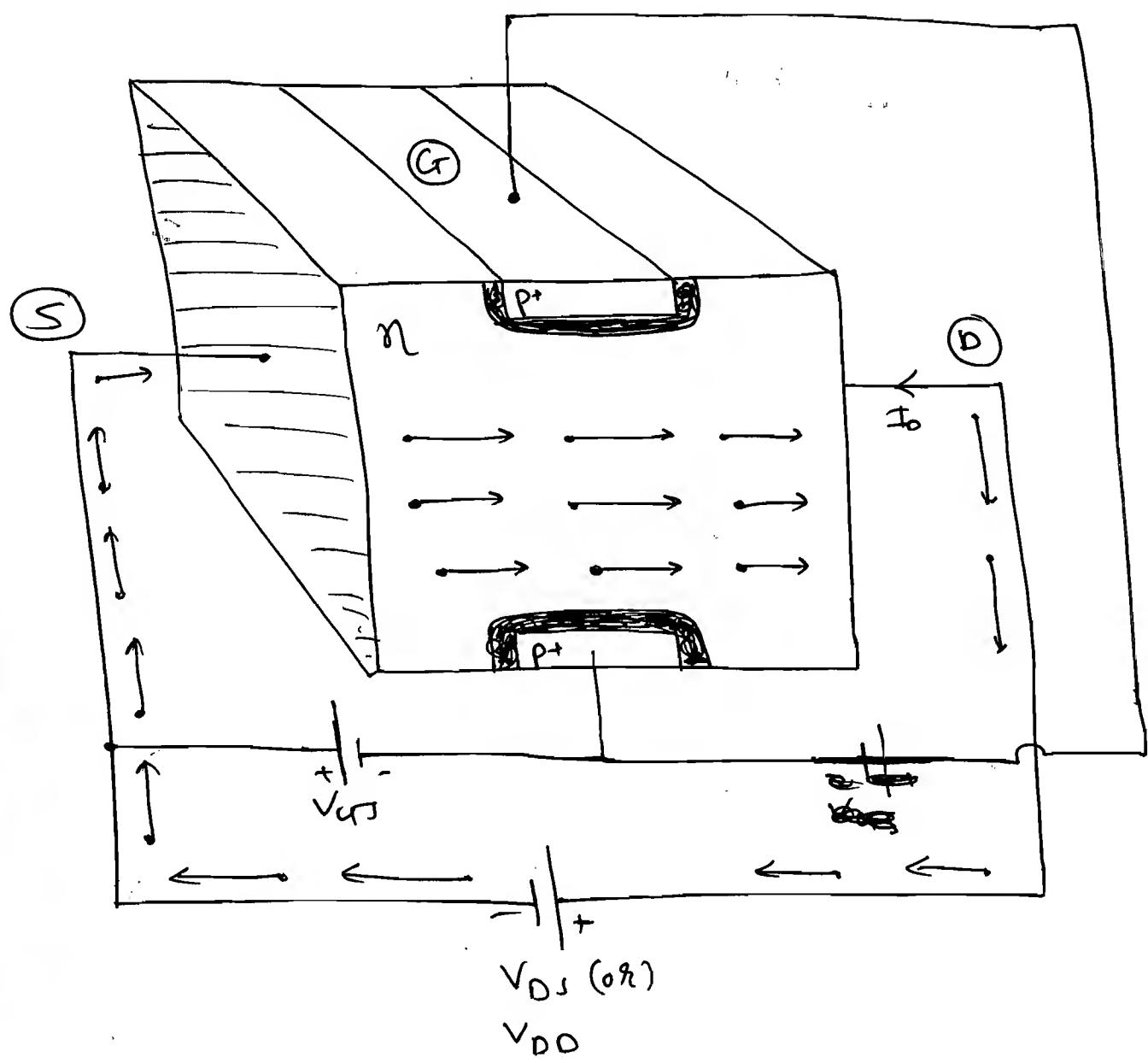
⇒ As transistor shrinks i.e. reduction in size it becomes faster & consumes less power.



*

n-Channel

JFET:



$$\rightarrow I = \frac{Q}{T} \Rightarrow I = \frac{Qn}{T}$$

$$I = \frac{Nq}{T}$$

① Source:

\Rightarrow Source is the terminal through which majority carriers enter into the semiconductor bar.

* Drain:

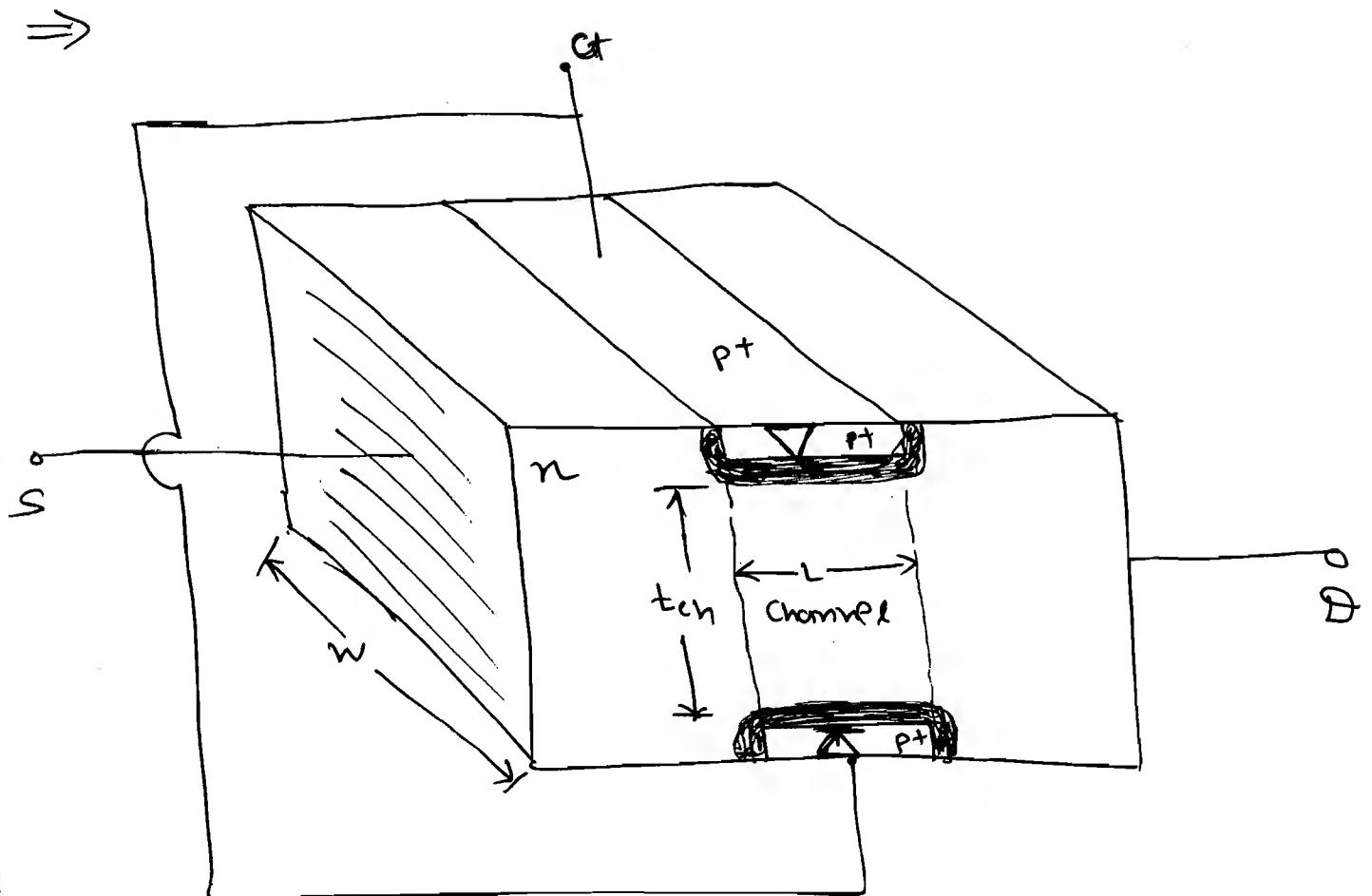
→ Drain is the terminal through which majority carriers are leaving from the semiconductor bus.

* Gate: (or):

⇒ Gate is the two heavily doped P^+ regions diffused both the sides of the bus and it controls the flow of carriers, (or) current betⁿ source and drain.

* Channel:

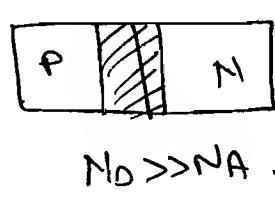
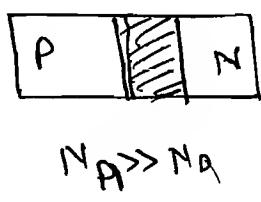
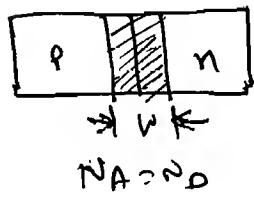
⇒ Channel is the region betⁿ two heavily doped P^+ gate region through which carriers moves from source to drain.



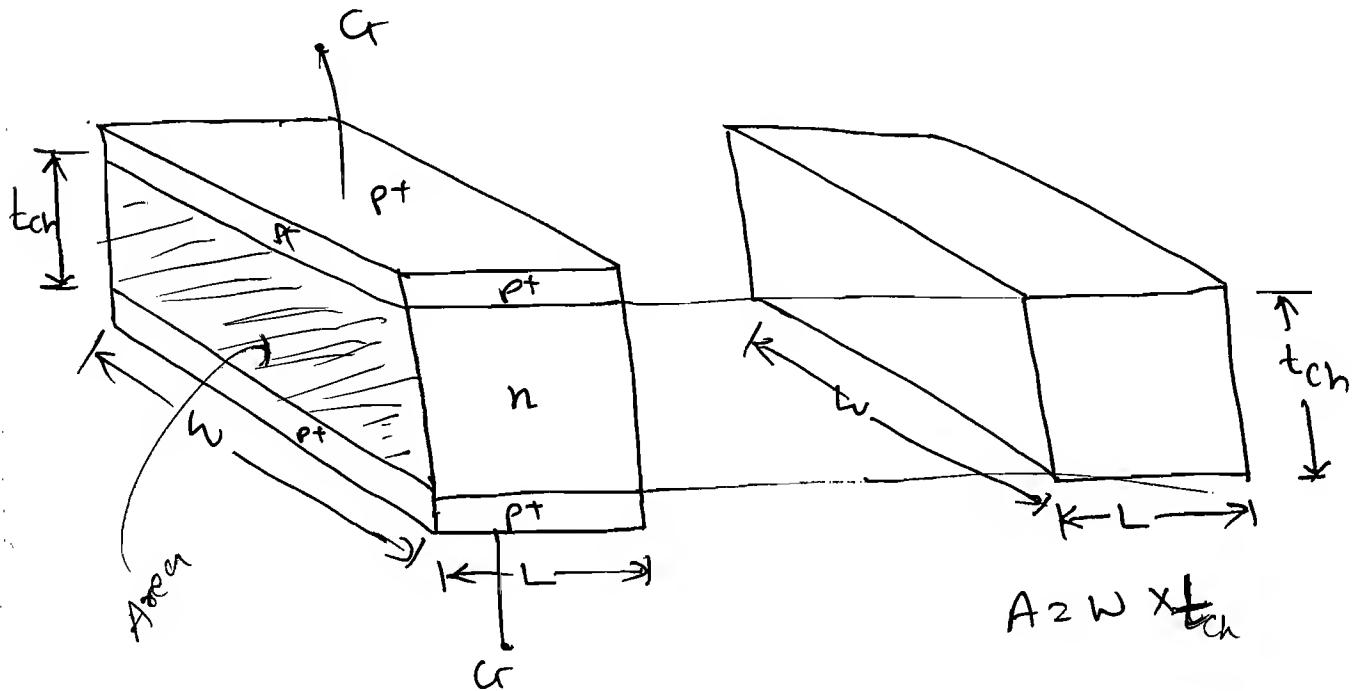
$$V_j = V_0$$

$$I_D \text{ (or) } I_{DS} = 0.$$

$$C \propto \sqrt{\frac{1}{nA} + \frac{1}{n_D}}$$



\Rightarrow Channel Position:



$$A = W \times t_{ch}$$

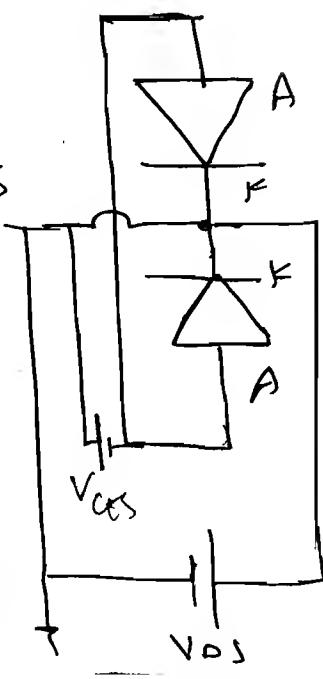
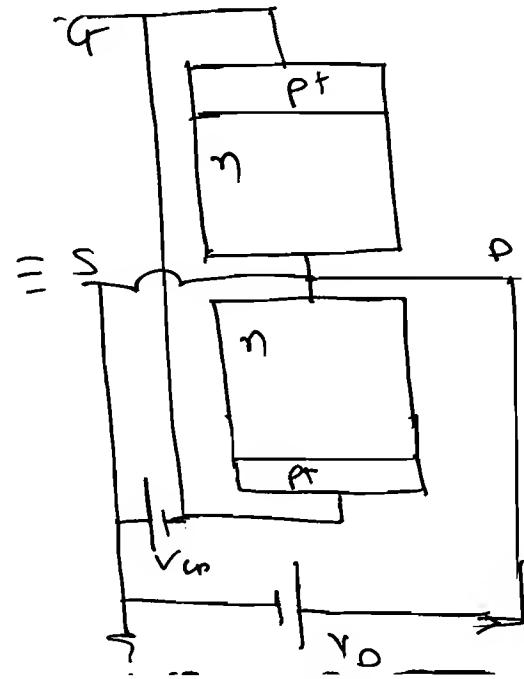
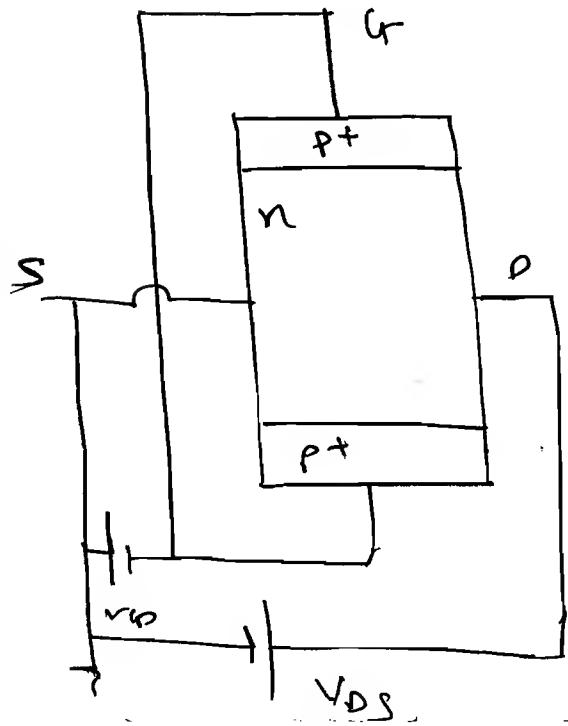
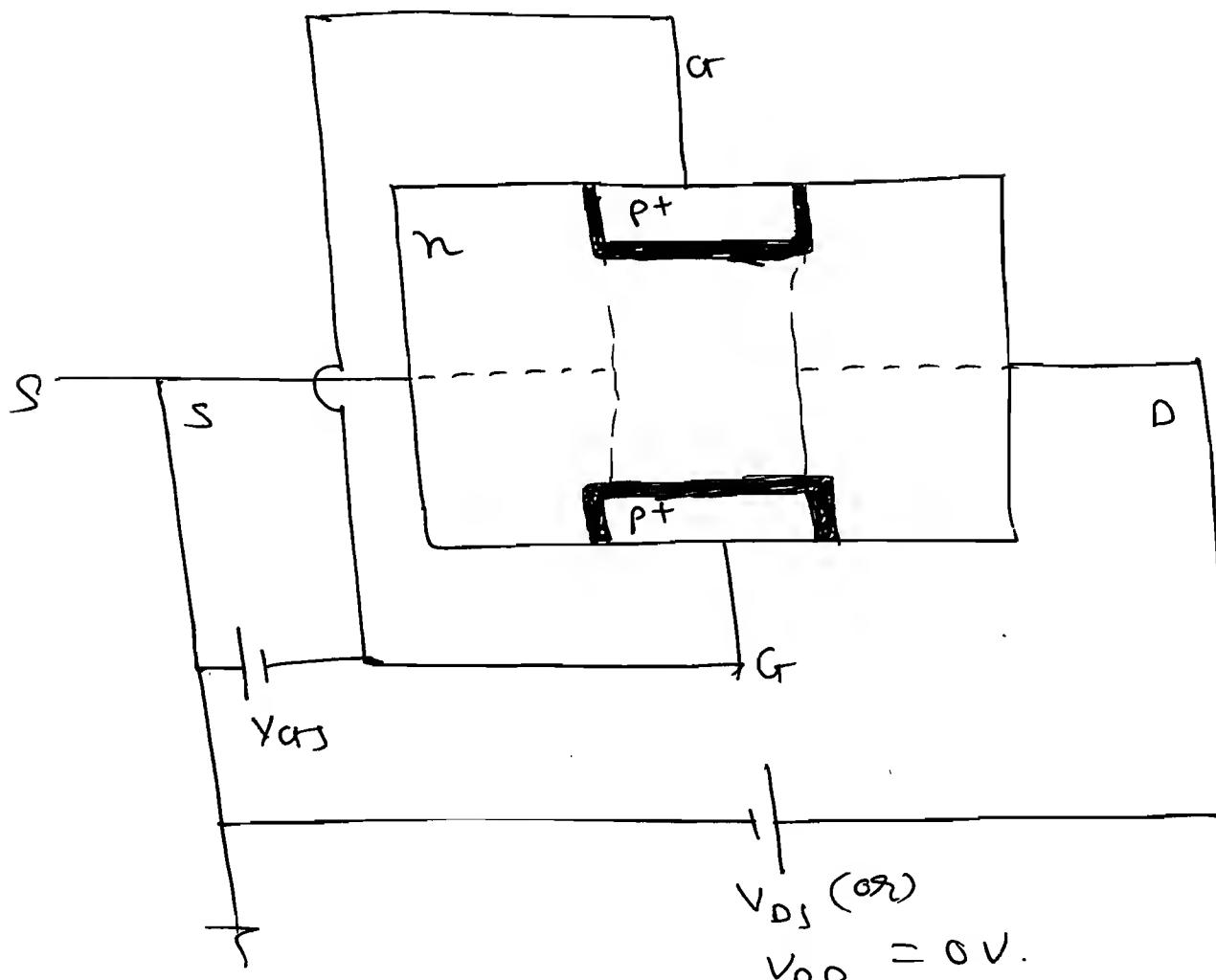
$$\rightarrow R = \frac{\rho L}{A}$$

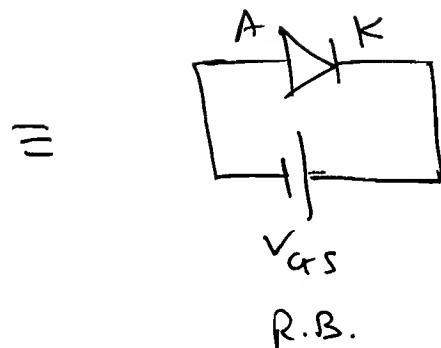
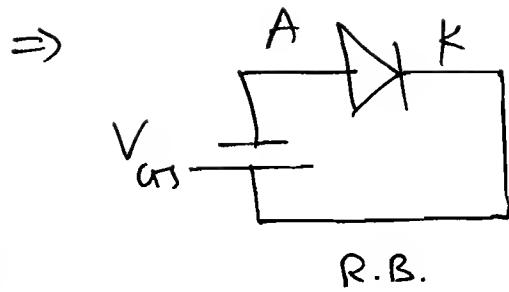
$$R_n = \frac{1}{n e n^2} \approx \frac{1}{N_0 e n^2}.$$

$$R_{ch} = \frac{\rho L}{A}$$

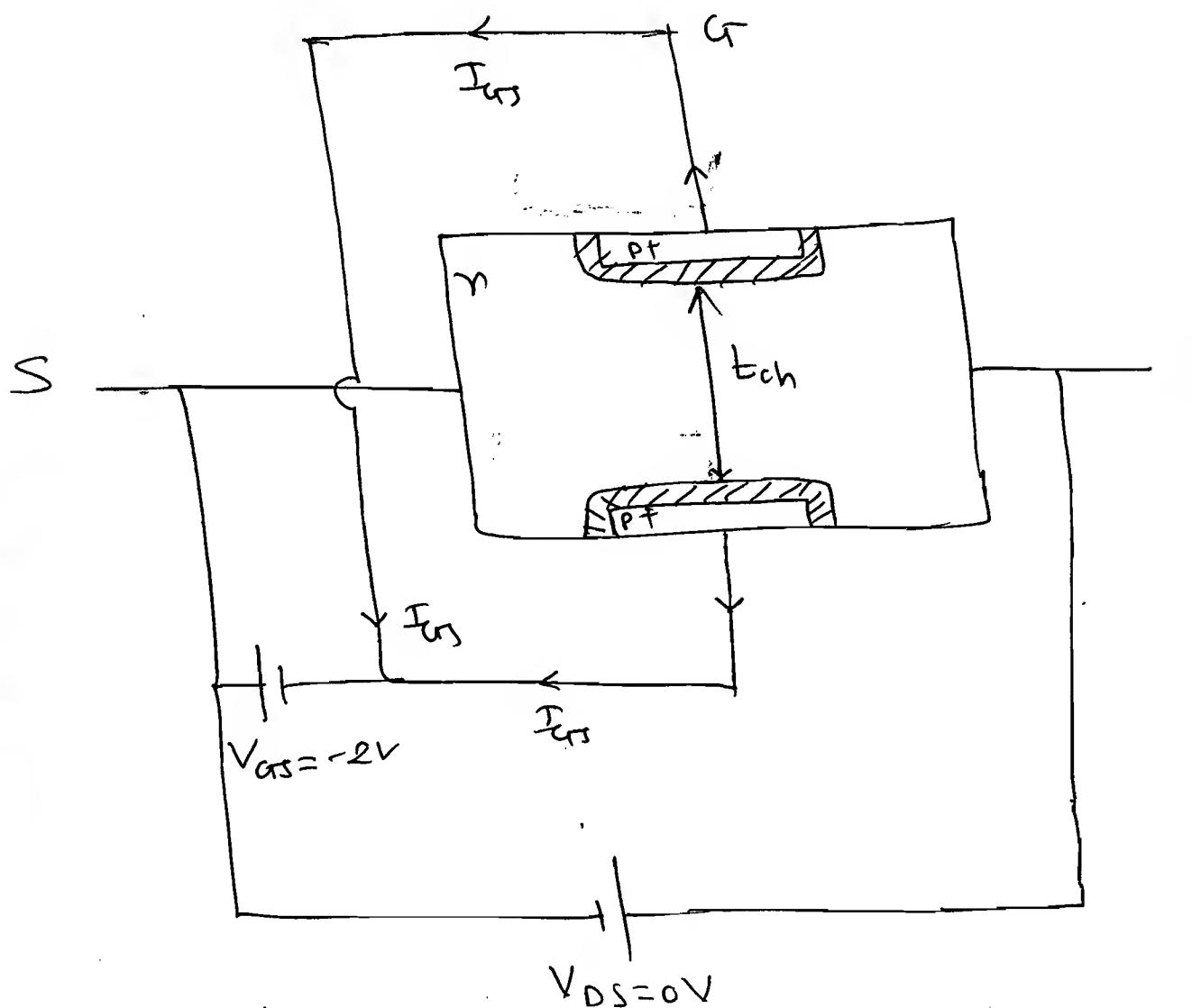
$$\text{Let, } R_{ch} = 500 \Omega.$$

\Rightarrow





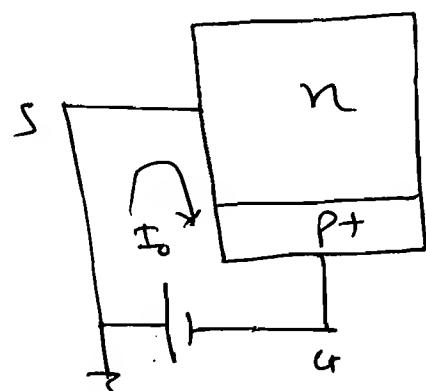
\Rightarrow When $V_{GS} = -2V$ & $V_{DS} = 0V$



$$V_j = V_0 + V_{GS}$$

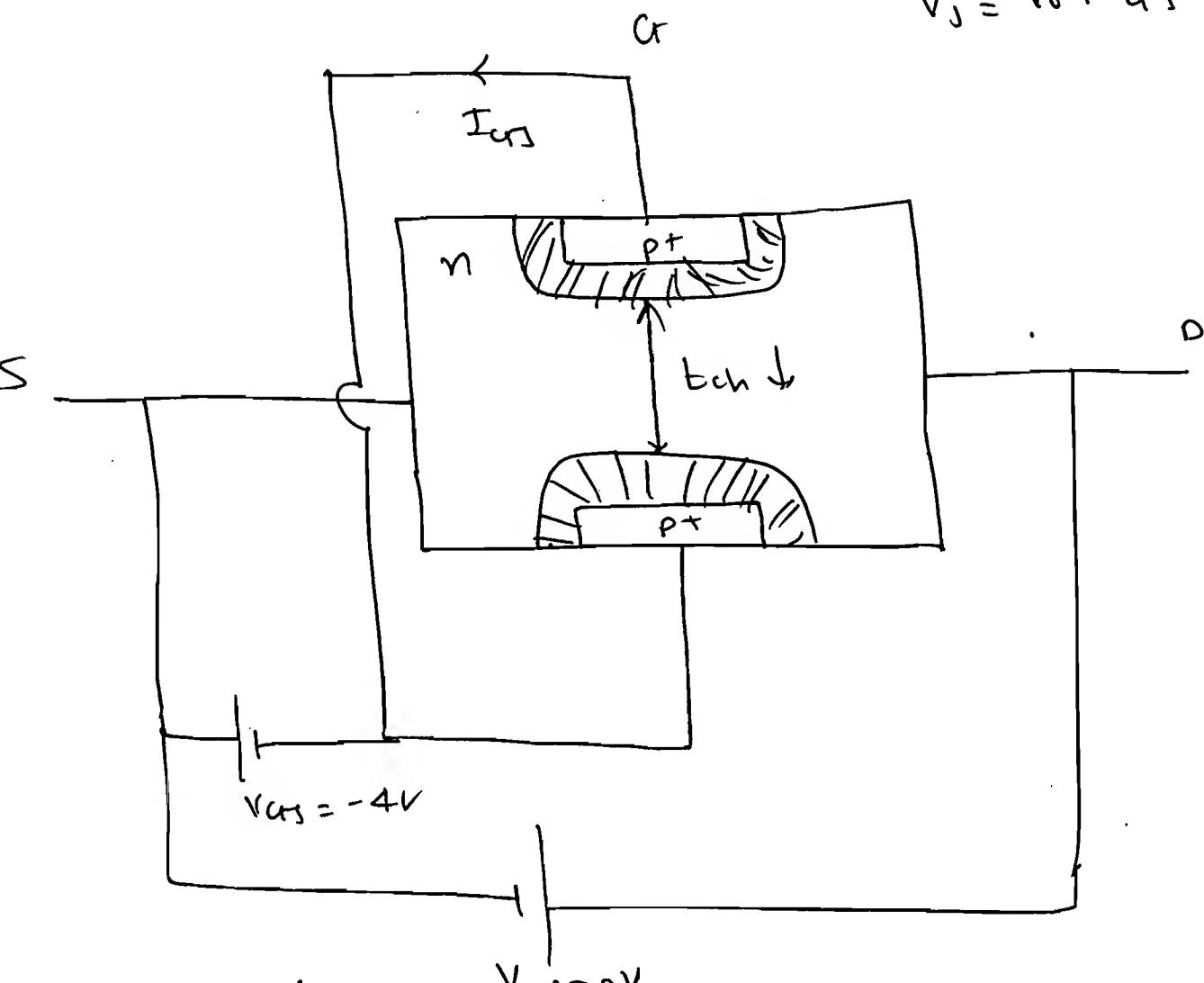
$$A \downarrow = w \times t_{ch} \downarrow$$

$$R \uparrow = \frac{S_L}{A \downarrow}$$



10) \Rightarrow When $V_{GS} = -4V$.

$$V_J = V_0 + V_{GS}$$

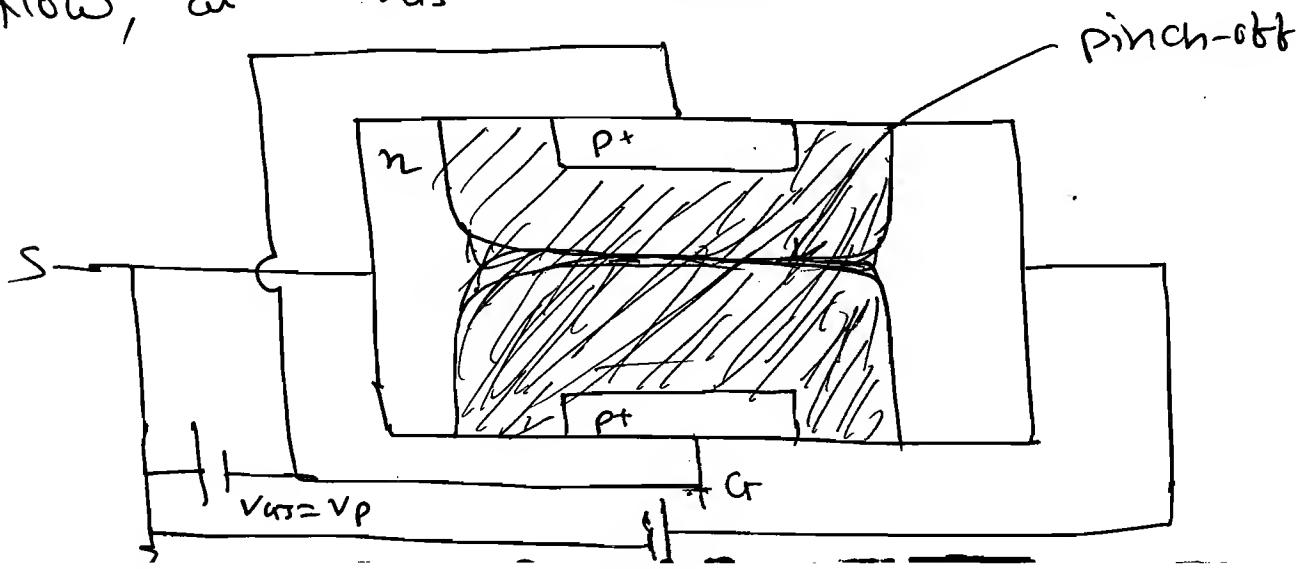


$$A \downarrow = w \times tch \downarrow$$

$$IRF \frac{SL}{A \downarrow}$$

\Rightarrow So, this JFET can be used as Voltage Regulator Variable Resistor.

Now, at $V_{GS} = V_{GS(\text{cutoff})} = V_p$.



$$V_j = V_o + V_{oss} (\text{cut-off}).$$

$$\Rightarrow t_{ch} = 0 \Rightarrow A = w \times t_{ch} \approx 0 \text{ m}^2.$$

$$\Rightarrow R = \frac{SL}{A} = \infty \text{ }\Omega.$$

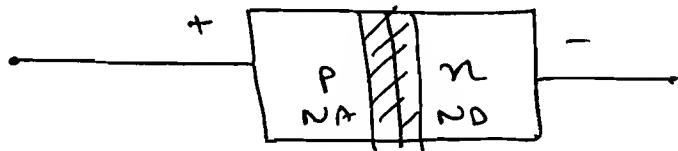
$$\Rightarrow R_{ch} = \infty \Omega \text{ so. open circuit.}$$

i.e. JFET is off or in cut-off.
 I_d

\Rightarrow At particular value of V_{oss} , thickness of the channel is almost zero and no carrier is flow from source to drain end hence no current flow and JFET comes into cut-off. This condition is called pinch-off. and (it range) from -9V to -25V.

\Rightarrow O.C.

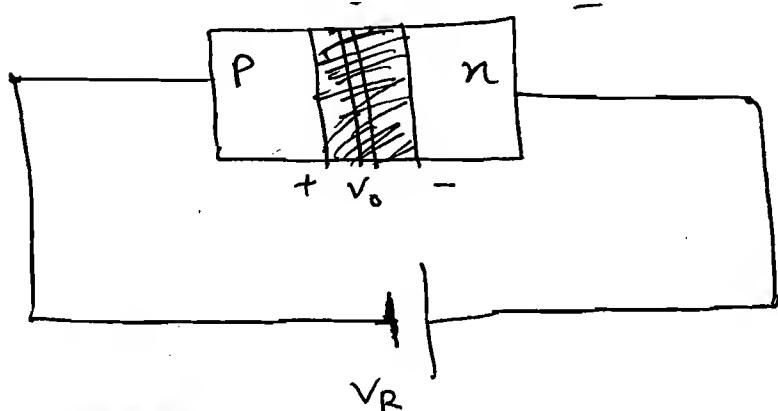
$$V_o = V_j$$



$$V_j = V_o$$

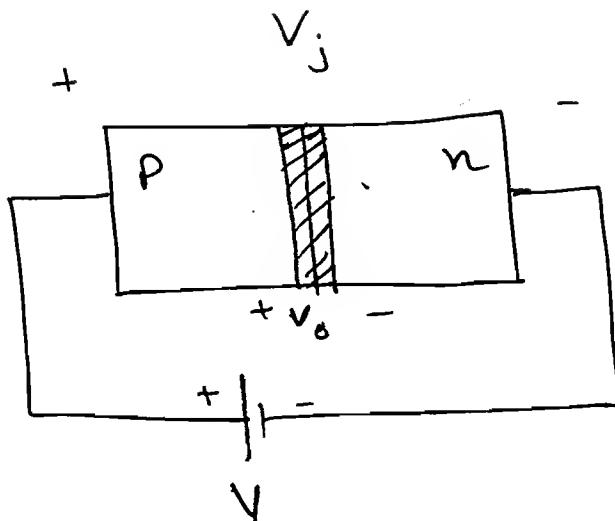
\Rightarrow R.B.

$$V_j$$



$$V_j = V_0 + v_R.$$

$$\Rightarrow \underline{F.B.}$$



$$\therefore \text{By KVL, } V - V_j - V_0 = 0.$$

$$\therefore V_j = V - V_0.$$

$$V_j = V_0 - V_F.$$

$$\Rightarrow V_{GSS}(\text{cut-off}) = V_{GSS}(\text{on}) = V_p.$$

\Rightarrow Condition for Pinch-off:

$$\therefore V_{DS} = V_{GSS} - V_p.$$

$$\therefore 0 = V_{GSS} - V_p \Rightarrow V_{GSS} = V_p = -10V.$$

$$\Rightarrow I_{GSS} \rightarrow nA$$

- I_{GSS} : Reverse Saturation Current
- : Depend on temp.
- : Inc by $7 \cdot 10^{-3} / {}^\circ\text{C}$.
- : Double 10°C .

I_{GSS} at T_1 (given)

I_{GSS} at T_2 = ?

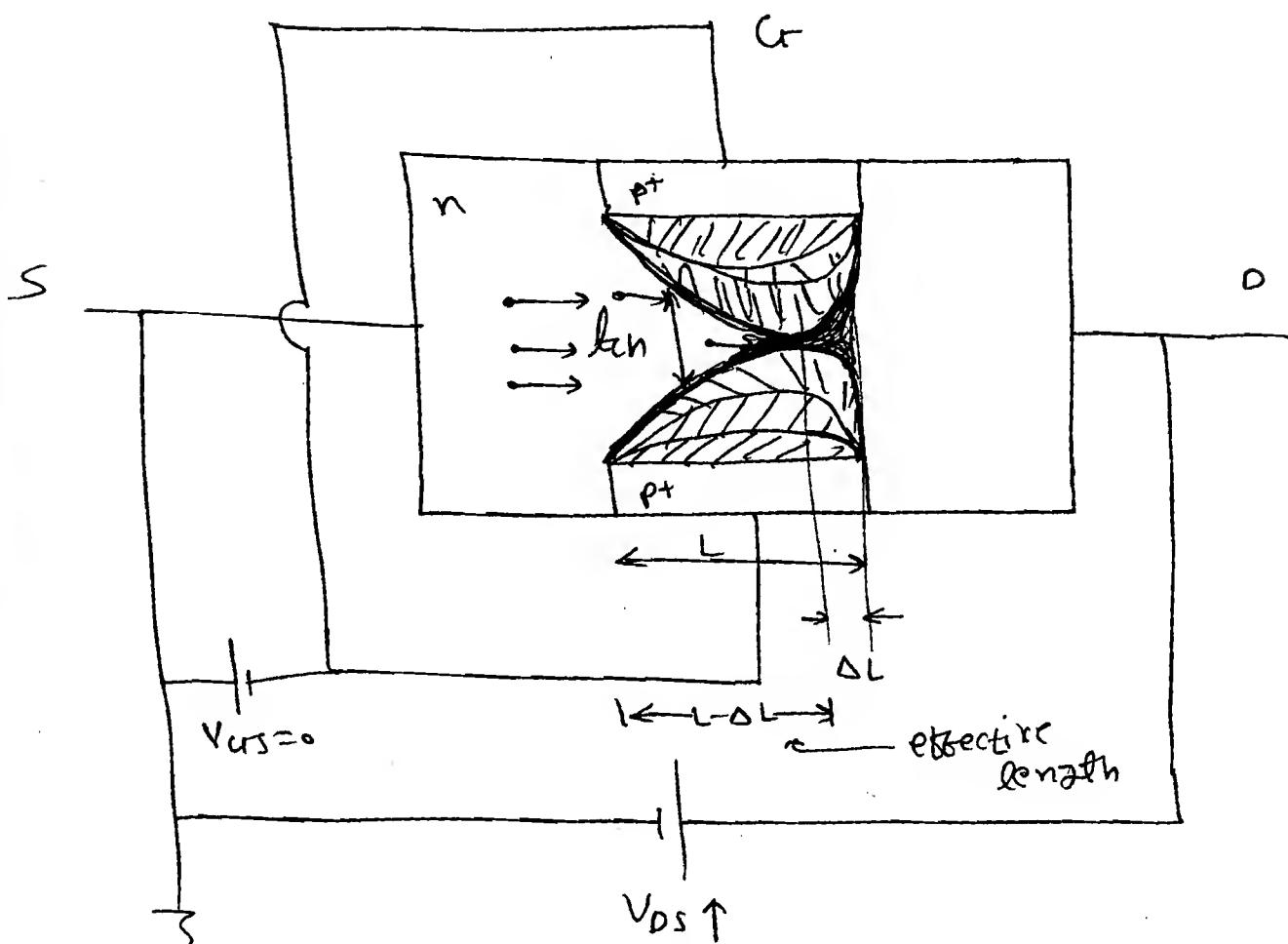
$$I_{GSS}(T_2) = 1$$

⇒

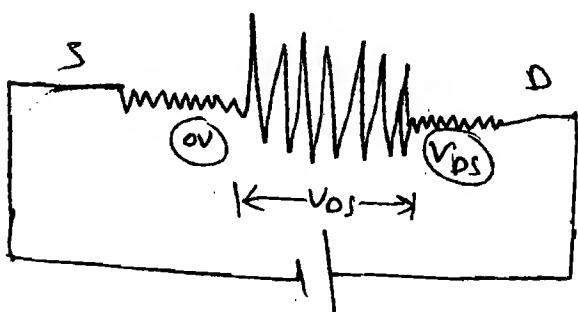
$$I_{GSS}(T_2) = \frac{1}{2} \cdot \frac{(T_2 - T_1)}{10} \cdot I_{GSS}(T_1)$$

$$I_{D2} = \frac{1}{2} \cdot \frac{(T_2 - T_1)}{10} \cdot I_{D1}(T_1)$$

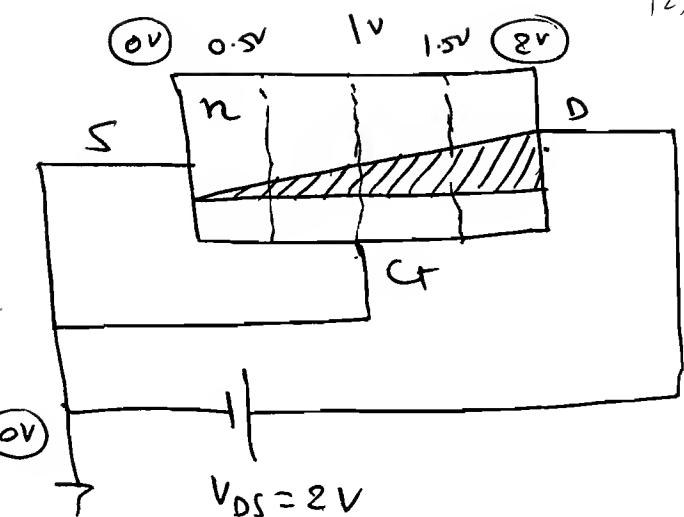
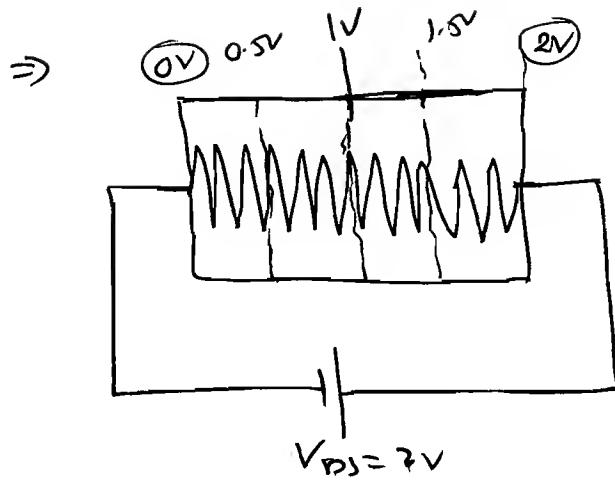
Case - ii Now, $V_{GS} = 0$,



⇒ Resistance across the channel:



When we move from Source to Drain Channel resistor is increased.



$$\Rightarrow E \uparrow = \frac{V_{DS}}{L} \uparrow$$

$$V \propto E$$

$$\Rightarrow V_{DS} \propto E$$

$$\Rightarrow I_{DS} \propto V_{DS}.$$

* Condition for Pinch-off:

$$\Rightarrow V_{DS} = V_{GS} - V_P.$$

$$\therefore V_{DS} = 0 - V_P$$

$$V_{DS} = -V_P = -(-10) = 10V.$$

$$\Rightarrow E = \frac{\Delta V_{DS}}{\Delta L}$$

\Rightarrow At ΔL position E is constant.

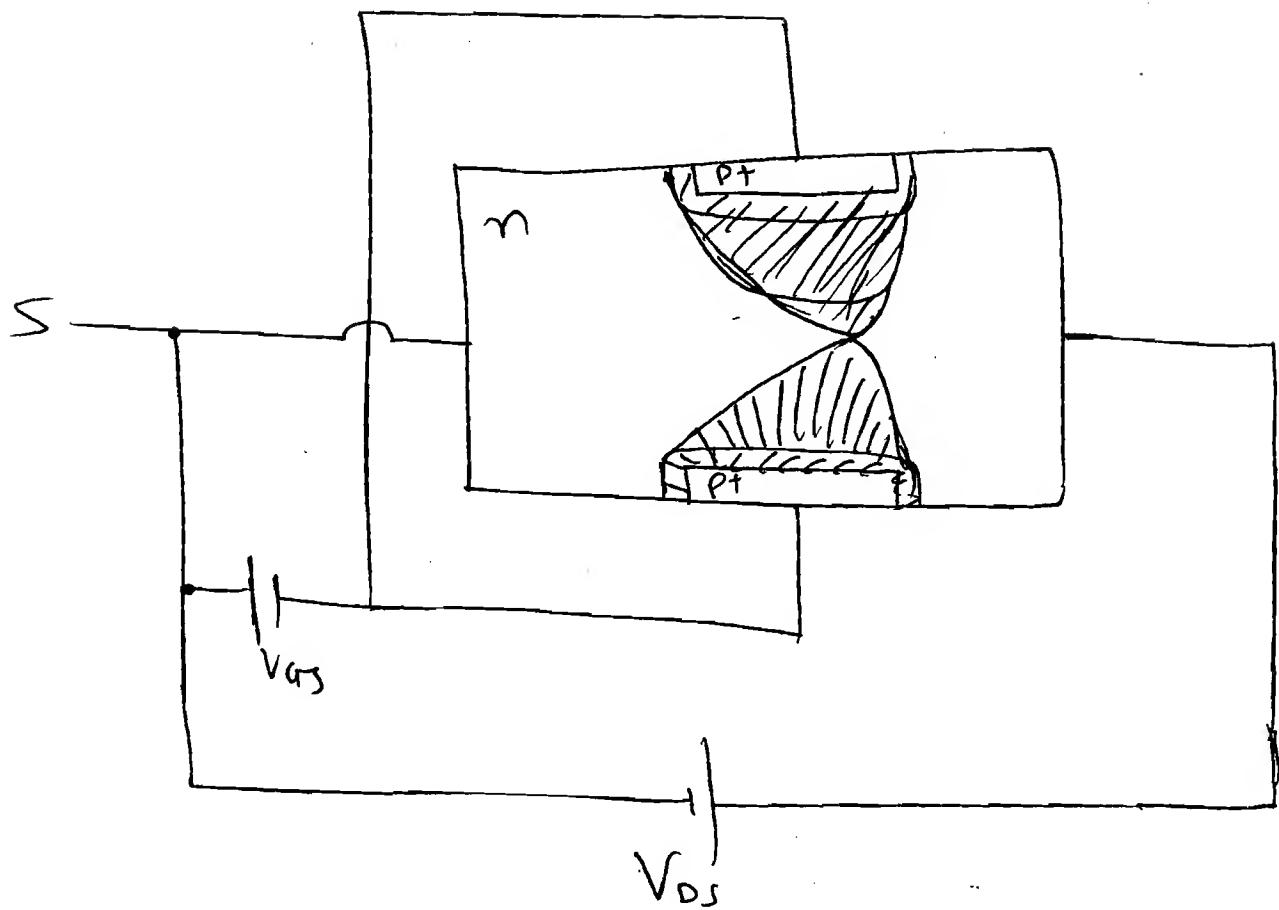
$$\Rightarrow I_D \text{ (or) } I_{DS} = I_S.$$

$$\Rightarrow V_J = V_0 + V_{GS} + V_{DS}.$$

Note: In BJT we decide region of operation based on biasing of BE and CB junction. In JFET we will decide the region of operation based on the I_D current. In Sat' region

I_D remains constant.

\Rightarrow



$$V_J = V_0 + V_{GS} + V_{DS},$$

$$\Rightarrow V_{DS} = V_{GS} - V_P.$$

$$V_{GS} - V_P = -2V - (-10V) = 8V.$$

if $V_{DS} = 8V$

$$\Rightarrow V_{DS} = V_{GS} - V_P$$

if $V_{DS} = 7V$

$\Rightarrow V_{DS} < V_{GS} - V_P \Rightarrow$ operate in linear region.

if $V_{DS} = 10V$

$\Rightarrow V_{DS} > V_{GS} - V_P \Rightarrow$ operate in sat. region.

$$V_P = -10V$$

$$V_{GS} = -10$$

$$V_P = -10V$$

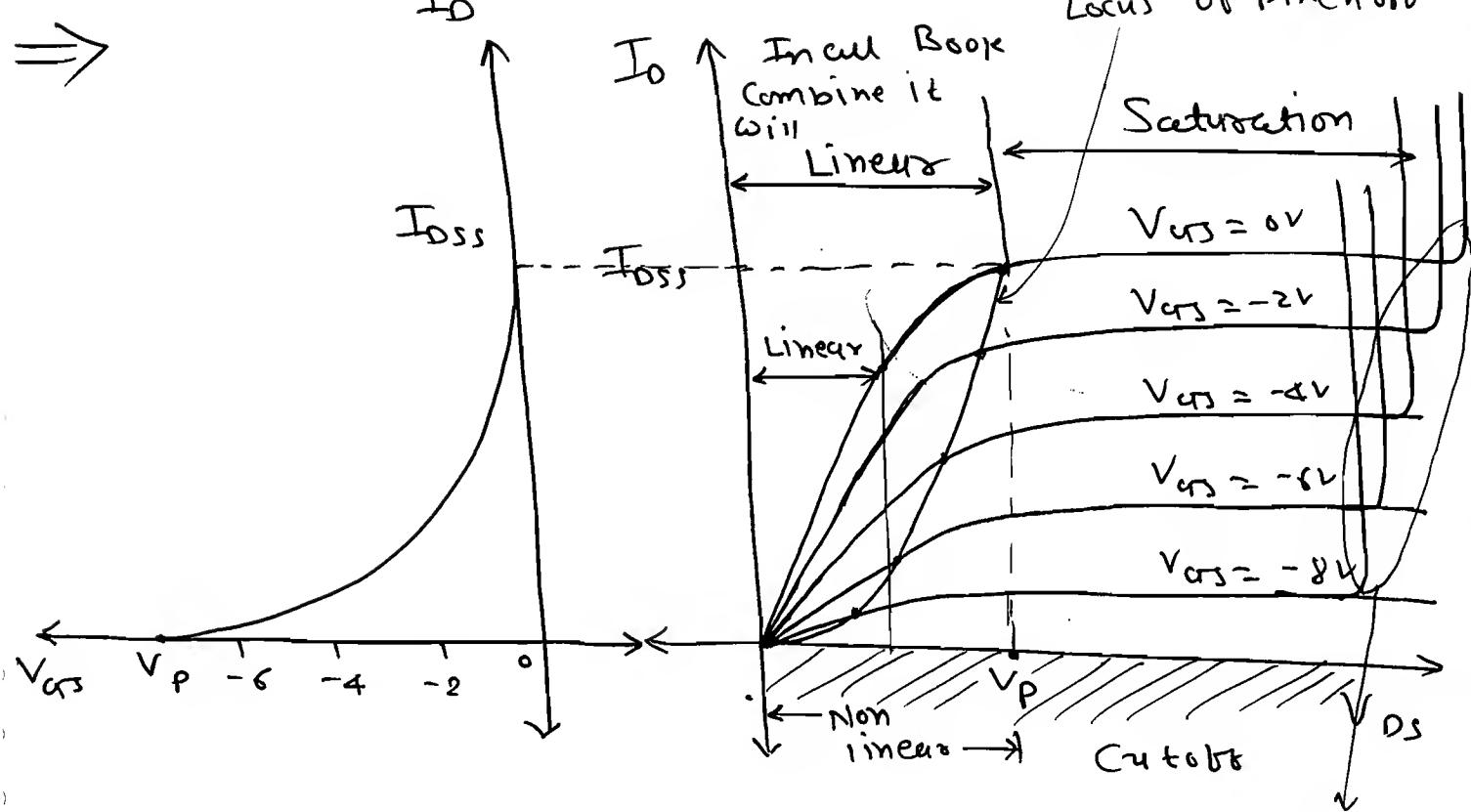
$$V_{GS} = -12$$

$$V_{GS} = V_P$$

$$V_{GS} < V_P$$

$$V_{GS} < V_P$$

$V_{GS} \leq V_P \Rightarrow$ cut-off.



(Transfer characteristics)

(Drain characteristics)

⇒ To find the region of operation

V_{GS} , V_{DS} & V_P should be known.

→ if $V_{GS} \leq V_P \rightarrow$ Cut-off

→ $V_P < V_{GS} < 0$.

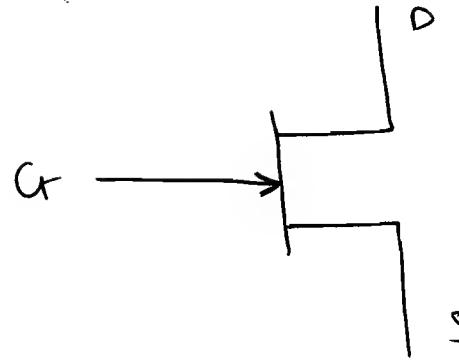
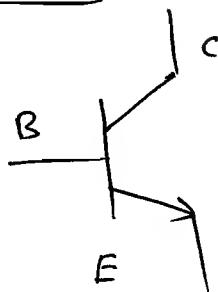
Calculate $V_{GS} - V_P$:

- if $V_{DS} < V_{GS} - V_P$ = linear
- if $V_{DS} > V_{GS} - V_P$ = Saturation.

⇒ BV_{DS} = Drain to Source breakdown voltage.

* Symbol:

⇒ BJT:



Same concept as in
BJT

Direction of arrow

decided Based on

emitter current.

for npn it leaves

and pnp it enters

to the Base.

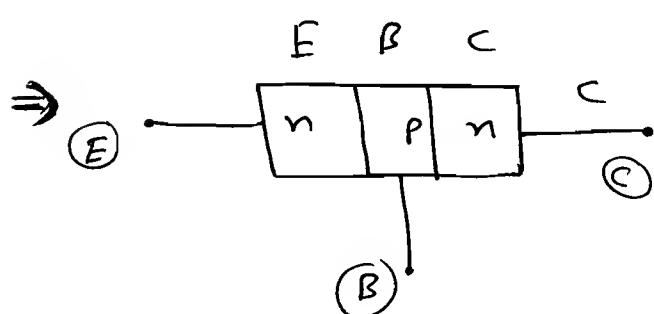
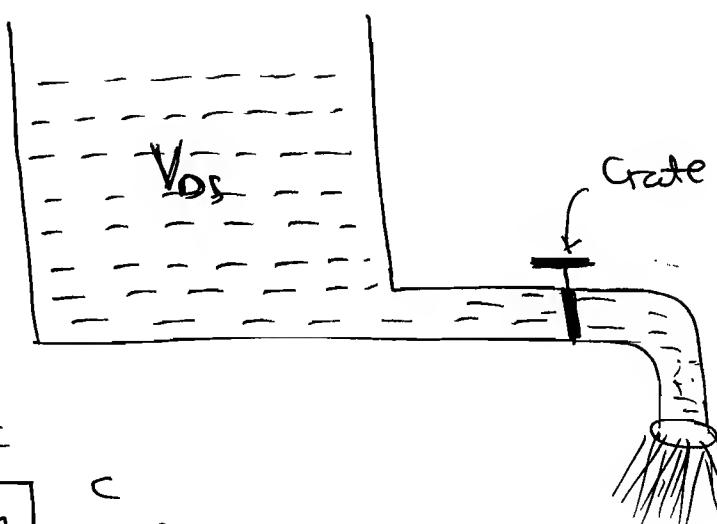
→ At $V_{GS} = 0 \Rightarrow I_D = I_{DSs}$

→ $I_D \leq I_{DSs}$

→ At $V_{GS} = 0$

$I_S = I_D = I_{DSs}$.

⇒



⇒ BJT is not a ~~uni~~ bilateral device. It

is a ~~bi~~ unilateral device. because if we

change ^{polarity} of supply the current will not sum.

because in BJT Carrier Concentration is not

same in C & E. In BJT Collector is collector

Emitter is omitted.

14)

⇒ Where as in JFET drain and source can be interchanged.

⇒ V_g then

* Important points to be remember in n-channel JFET.

⇒ n-Channel JFET operates with -ve gate to source voltage. i.e. -ve V_{GS} values

⇒ Gate to source voltage and pinch-off voltages are -ve for n-channel JFET.

⇒ n-JFET operates in depletion mode for -ve V_{GS} values.

⇒ JFET operates always in depletion mode.

⇒ JFET operates with reversed biased gate junction.

⇒ $V_{GS(\text{cut-off})}$ voltage is the value of the V_{GS} at which both the gate depletion regions comes close and the thickness of the channel becomes zero and also drain current $I_D = 0$. ($V_{DS} = 0$).

⇒ pinch-off voltage is the minimum value of V_{GS} at which drain ~~current~~ current

becomes constant. ($V_{DS} = 0$).

⇒ The relation betⁿ V_{DS} (cut-off) Voltage and V_p is

$$V_{DS(\text{cut-off})} = V_{DS(\text{sat})} = V_p.$$

⇒ In n-channel JFET as V_{DS} decreases (i.e. increasing in -ve direction) pinch-off voltages happens for lower values of V_{DS} .

⇒ Condition for pinch-off (or) Saturation is

$$V_{DS} = V_{DS} - V_p$$

(+ve) (-ve) (-ve)

⇒ In n-JFET as V_{DS} increases avalanche break-down happens due to avalanche effect for lower values of V_{DS} .

⇒ JFET operates in linear, saturation and cut-off region.

⇒ Linear region is the region which is left side to the pinch-off locus.

⇒ Sat. region is the region Right side to the pinch-off locus.

⇒ Cut-off region is the region below $V_{DS} = V_p$.

\Rightarrow JFET can be used as Amplifier in¹⁵⁾ a Sat. region and it can be used as a switch in a linear and cut-off regions.

\Rightarrow JFET can be used as Voltage Variable Resistor in linear region and it can be operate as current source in saturation region.

\Rightarrow Linear region is also called 'Ohmic region' (or) triode region.

\Rightarrow Transfer char. of a JFET gives pinch-off voltage (V_p), I_{oss} and transconductance (g_m).

\Rightarrow For $V_{GS} \leq V_p$ n-channel JFET operates in cut-off region and its drain current $I_D = 0A$.

\Rightarrow For $V_p < V_{GS} < 0$ & $V_{DS} < V_{GS} - V_p$ it operates in linear region and its drain current

$$\therefore I_D = \frac{2 I_{oss}}{V_p^2} \left[(V_{GS} - V_p) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

↓-ve ↓-ve ↑+ve

\Rightarrow For $V_p < V_{GS} < 0$ and $V_{DS} \geq V_{GS} - V_p$ it operates in sat. region. and its drain current

$$I_D = I_{oss} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

↓-ve ↓-ve

Note:

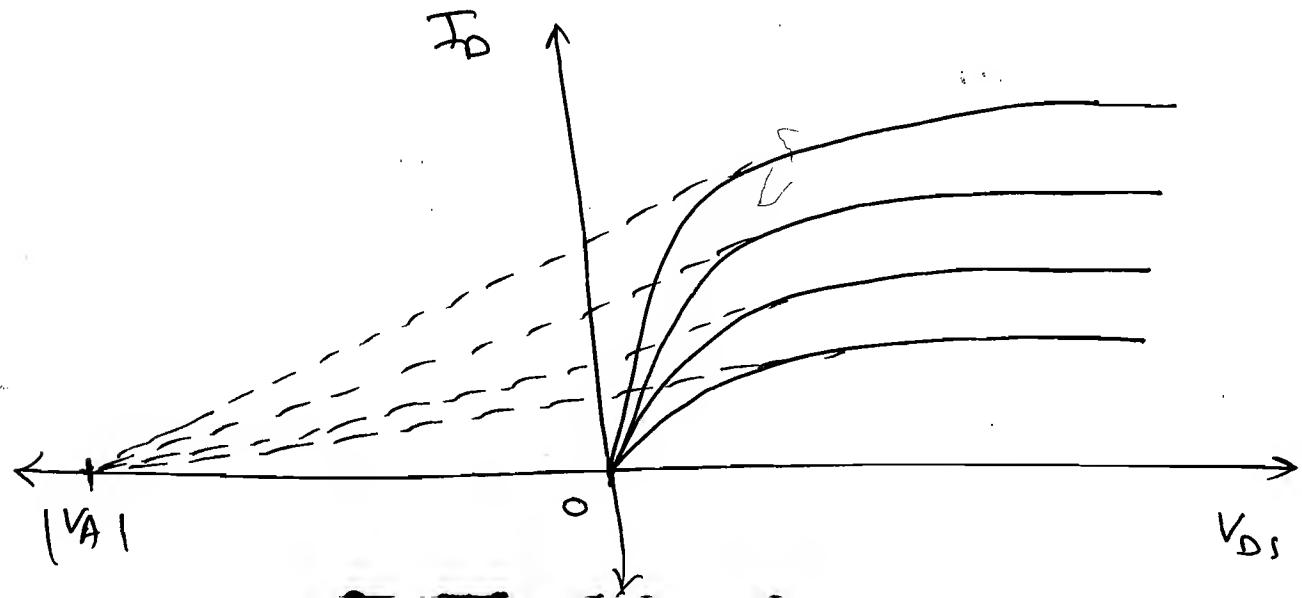
⇒ JFET is a symmetrical device therefore Source and Drain terminal can be interchanged.

* Channel Length Modulation

⇒ In saturation region of drain to source voltage increases the effective length of the channel is decreases i.e. as V_{DS} varies, the length of the channel is also varies. i.e. called channel length modulation. Due to channel length modulation drain current increases as

$$I_D = I_{DSS} \left[1 - \frac{V_{DS}}{V_P} \right]^2 (1 + \lambda V_{DS})$$

where, λ is channel length modulation parameter. $\lambda = \frac{1}{V_A}$, V_A = early voltage.



* DRAIN Resistance (or) o/p resistance: 16

⇒ It is the Resistance offered by the JFET in the Sat. region.

⇒ It is the reciprocal of the slope of drain characteristics in the Sat. saturation region.

$$\Rightarrow \gamma_d \text{ (or) } \gamma_o = \frac{1}{\frac{\Delta I_o}{\Delta V_{DS}} \Big|_{V_{DS}}} = \frac{dV_{DS}}{dI_o} \Big|_{V_{DS}}$$

⇒ Drain Resistance (or) o/p Resistance are also called Ac resistance (or) small signal resistance.

$$\Rightarrow \gamma_d \text{ (or) } \gamma_o = \frac{1}{\lambda I_o} = \frac{V_A}{I_o} \quad (\because \frac{1}{\lambda} = V_A).$$

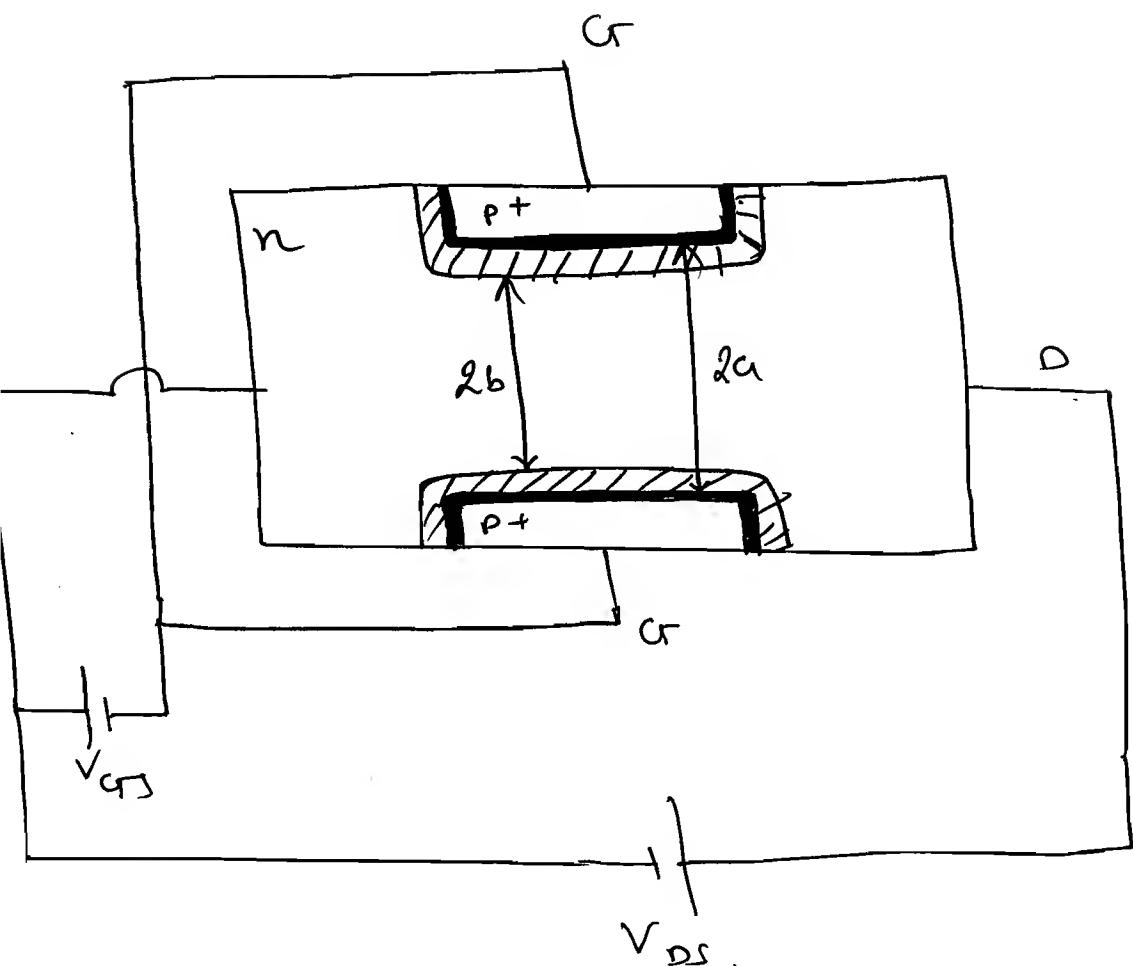
→ It ranges from $50\text{ k}\Omega$ to $100\text{ k}\Omega$.

* Transconductance (g_m):

⇒ Transconductance is also called as mutual conductance (or) figure of merit.

⇒ It gives how effectively JFET converts Voltage changes at the input to the corresponding current changes at the o/p in the saturation region.

$$g_m = \frac{\Delta I_o}{\Delta V_{DS}} \Big|_{V_{DS}} = \frac{dI_o}{dV_{DS}} \Big|_{V_{DS}}$$



a = half - channel thickness (or) width at $V_{GS} = 0$ V.

b = half - channel thickness (or) width at a given V_{GS} .

Pinch-off Voltage $\approx a$ n-JFET

$$V_p = \frac{e N_D}{2 \epsilon} \cdot a^2 \Rightarrow V_p = -ve$$

$$e = -1.6 \times 10^{-19} C.$$

ϵ = Permittivity of Si

$$\epsilon_r = \epsilon_0 \epsilon_r$$

$$\epsilon_r = 11.7 \approx 12$$

$$\epsilon_0 = 8.85 \times 10^{-12} F/m.$$

$$\epsilon_0 = 8.85 \times 10^{-14} F/cm.$$

a = half - channel thickness
at $V_{GS} = 0$.

⇒ Pinch-off Voltage of a P-JFET:

$$\rightarrow V_p = \frac{e N_A}{2 \epsilon} \cdot a^2$$

$e = 1.6 \times 10^{-19}$ C = charge of hole

N_A = acceptor Concentrate.

$$V_p = +ve$$

* Relation B/W V_{GS} & V_p :

$$\Rightarrow V_{GS} = [1 - b/a]^2 \cdot V_p.$$

$$\Rightarrow b = a \left[1 - \sqrt{\frac{V_{GS}}{V_p}} \right].$$

Ex-1 An n-channel JFET has channel thickness of 10μm at its channel thickness $V_{GS} = 0V$. Calculate at $V_{GS} = -5V$. Assume $V_p = -10V$.

So: Here, $2a = 10\mu m$ & $2b = ?$
 $V_p = -10V$

$$\therefore 2b = a \left[1 - \sqrt{\frac{V_{GS}}{V_p}} \right].$$

$$\therefore 2b = 2a \left[1 - \sqrt{\frac{V_{GS}}{V_p}} \right].$$

$$\therefore 2b = 10\mu \left[1 - \sqrt{\frac{-5}{-10}} \right]$$

$$\Rightarrow 2b = 10\mu \left[1 - \frac{1}{\sqrt{2}} \right]$$

$$2b = 2.93 \mu m.$$

= thickness of channel at $V_{GS} = -5V$.

* Drain ON Resistance (or) ON Resistance:

$$\Rightarrow \gamma_{d\text{on}} \text{ (or) } R_{d\text{on}} \text{ (or) } R_{\text{on}}$$

\Rightarrow It is the resistance offered by the JFET in linear region for small value of V_{DS} .

\Rightarrow It is the reciprocal of the slope of the drain characteristics in the linear region, for small value of V_{DS} .

$$\Rightarrow R_{\text{on}} = \left. \frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}} \right|_{V_{GS}} = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS}}$$

$$= \left. \frac{dV_{DS}}{dI_D} \right|_{V_{GS}}$$

$$\gamma_{d\text{on}} = \frac{L}{2\alpha w N \delta m^2 \left[1 - \sqrt{\frac{V_{GS}}{V_P}} \right]}$$

$\gamma_{d\text{on}}$ = Drain ON resistance at given V_{GS} .

$$\Rightarrow A_T = V_{GS} = 0V$$

$$\Rightarrow \gamma_{d_0\text{on}} = \left. \frac{L}{2\alpha w N \delta m^2} \right|_{V_{GS}=0}$$

$$\therefore \gamma_{d\text{on}} = \frac{\gamma_{d_0\text{on}}}{\left(1 - \sqrt{\frac{V_{GS}}{V_P}} \right)}$$

$\Rightarrow \gamma_{d\text{on}} > \gamma_{d_0\text{on}}$. it ranges from 100 Ω to 100 k Ω .

* Temperature effect:

\Rightarrow Case - (i) : V_p

V_p : dependent on Temp.
: Inc by $2.2 \text{ mV } ^\circ\text{C}$.

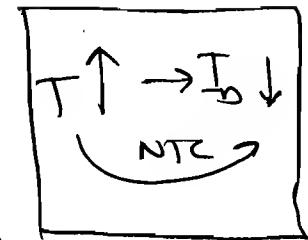
$$T \uparrow \rightarrow V_p \uparrow \rightarrow I_D \uparrow$$

PTC

PTC: +ve TEMP. Coefficient
(OR)

$$T \uparrow \rightarrow t_{ch} \uparrow \rightarrow R_{ch} \downarrow \rightarrow I_B \uparrow$$

PTC



\Rightarrow Case - (ii) : μ

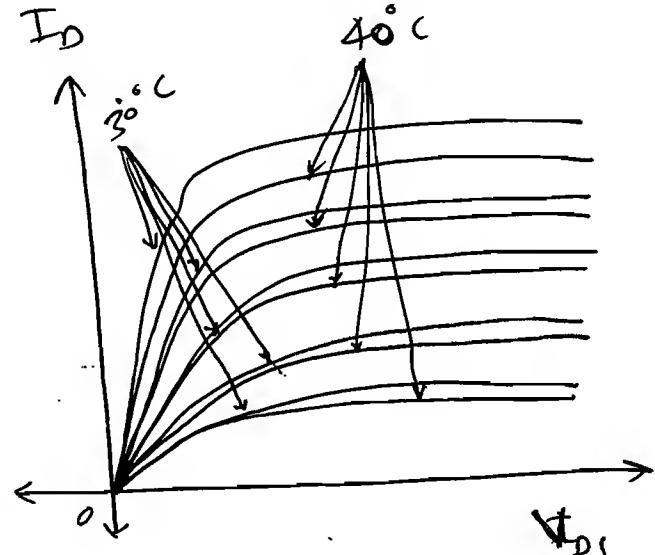
$$\mu \propto \frac{1}{T^m} \text{ (or) } \mu \propto T^{-m}$$

Si: $m = 2.5$ for ele. $\rightarrow \mu \propto \frac{1}{T^{2.5}}$
 $= 2.7$ for holes. $\rightarrow \mu \propto \frac{1}{T^{2.7}}$

Gre: $m = 1.66$ for ele.
 $= 2.33$ for holes.

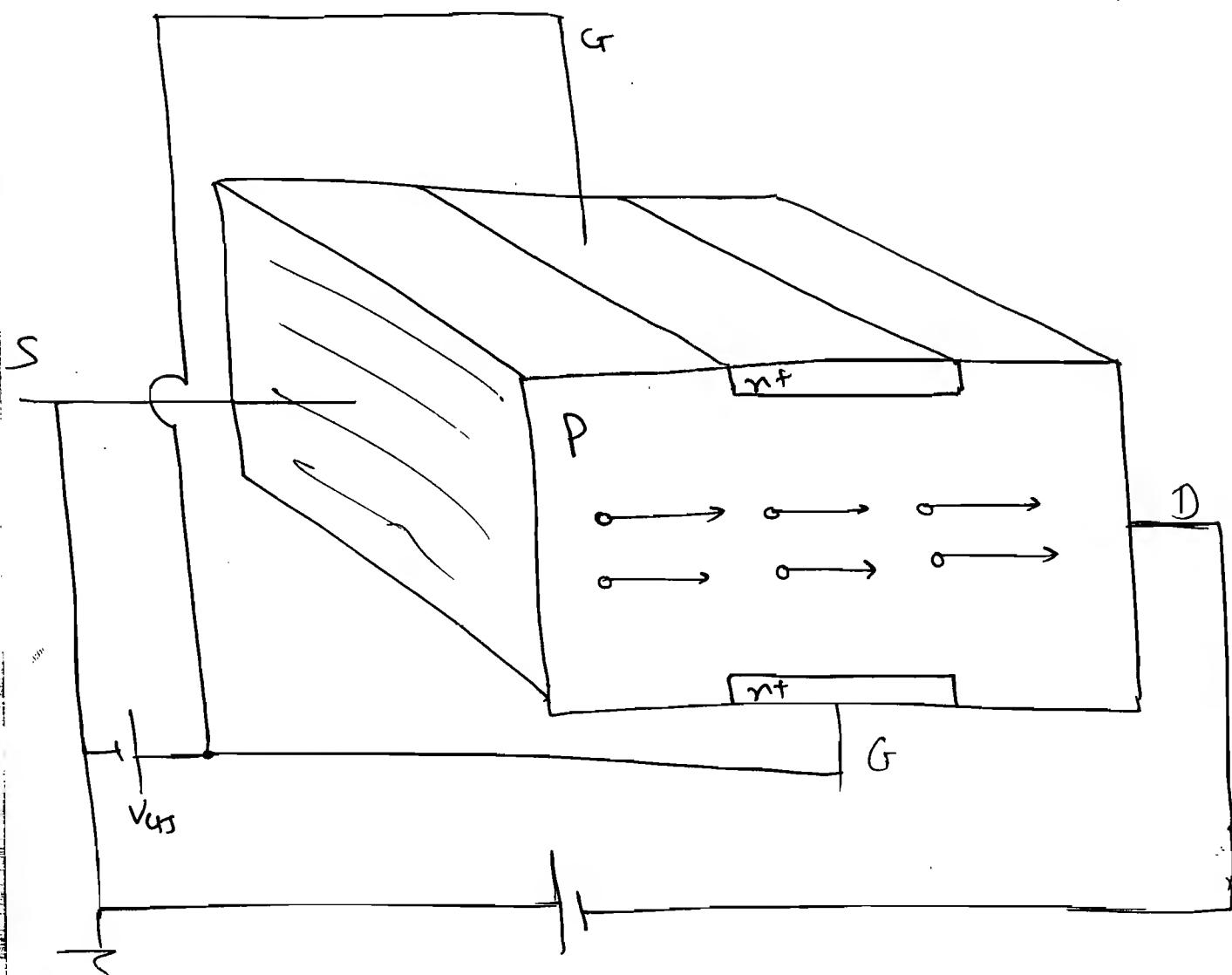
$$T \uparrow \rightarrow \mu \downarrow \rightarrow I_D \downarrow$$

NTC



* P- Channel

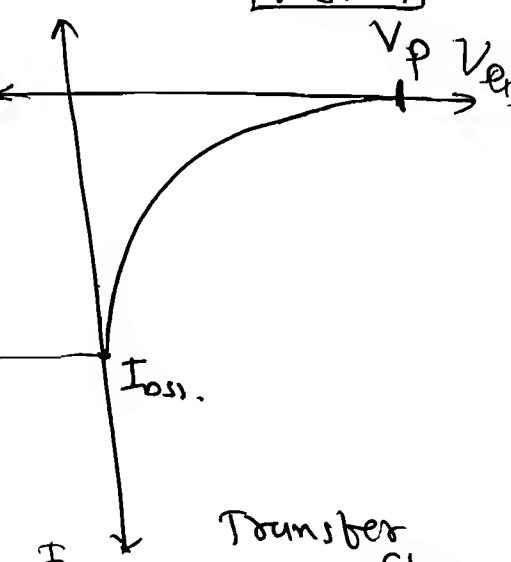
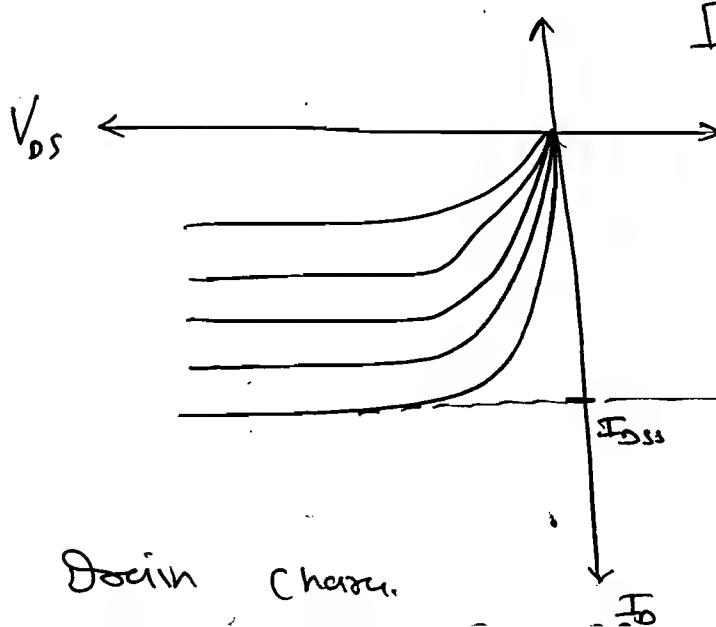
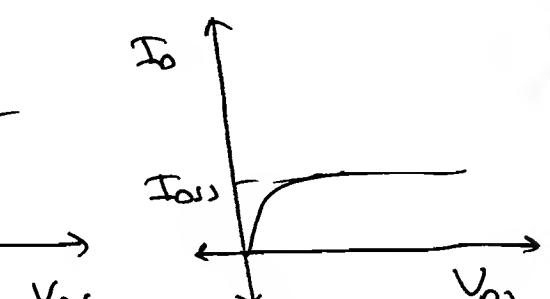
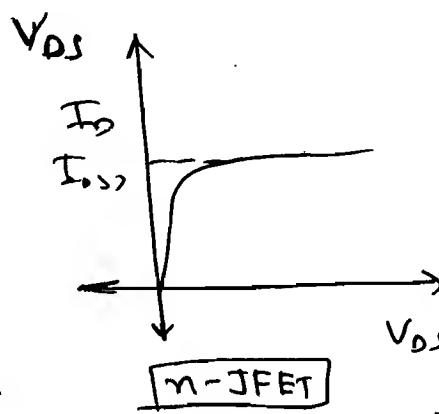
JFET:



V_{DS} = +ve

V_{GS} = +ve

V_P = +ve



$$\Rightarrow V_{DS} = V_{GS} - V_P.$$

↑ ↑ ↑
 -ve +ve +ve.

$$\left. \begin{array}{l} \text{let, } V_P = +10V \\ V_{GS} = 10V \end{array} \right\} V_{GS} = V_P = 10V \quad \left. \begin{array}{l} \\ \\ \end{array} \right\} V_{GS}$$

$$\left. \begin{array}{l} V_P = 10V \\ V_{GS} = 12V \end{array} \right\} V_{GS} > V_P$$

$0 < V_{GS} < V_P \rightarrow$ Linear (or) Sat.

$$V_{GS} - V_P = 2 - 10V = -8V$$

if $V_{DS} = -8V$

if $V_{DS} = -3V$

$V_{DS} > V_{GS} - V_P \Rightarrow$ linear region.

for $V_{DS} < V_{GS} - V_P \Rightarrow$ Sat. region.

* Imp. Points to be Remember for P-JFET:
 ⇒ P-channel JFET operates with +ve gate Voltages i.e. +ve V_{GS} values.

⇒ Gate to source Voltage (V_{GS}) and pinch-off Voltages (V_P) are +ve for P-JFET.

⇒ P-JFET operates in depletion mode for +ve V_{GS} values.

⇒ In P-JFET as V_{GS} increases pinch-off happens for higher values of V_{DS} .

\Rightarrow Condition for pinch-off (or) Sat.

$$V_{DS} = V_{GS} - V_p$$

↑ ↑ ↑
-ve +ve +ve

\Rightarrow In p-channel JFET as V_{GS} increases

Avalanche - Breakdown happens due to

avalanche effect for higher values of

V_{GS} .

\Rightarrow For $V_{GS} \geq V_p$ p-channel JFET operates in cut-off region and its drain current

$$I_D = 0.$$

\Rightarrow For $0 < V_{GS} < V_p$ & $V_{DS} > V_{GS} - V_p$ it

operates in linear region and its drain

current,

$$I_D = 2 \frac{I_{DSS}}{V_p^2} \left[(V_{GS} - V_p) V_{DS} - \frac{1}{2} V_{DS}^2 \right].$$

↑ ↑ ↑
+ve +ve -ve

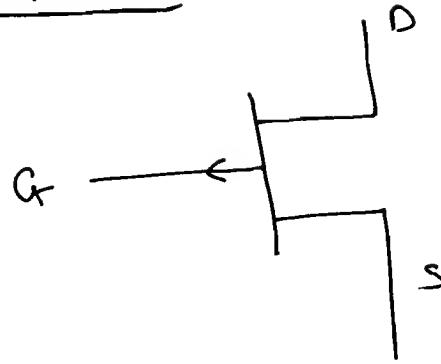
\Rightarrow For $0 < V_{GS} < V_p$ & $V_{DS} < V_{GS} - V_p$, it operates in ~~saturation~~ \Rightarrow saturation region and its drain current,

$$I_D = \frac{2 I_{DSS}}{V_p^2} \left[\frac{V_{GS}}{V_p} \right]$$

$$I_D = I_{DSS} \left[1 - \frac{V_{DS}}{V_p} \right]^2$$

↑
+ve

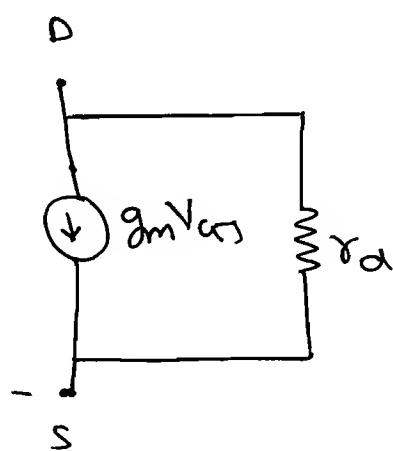
* Symbol :



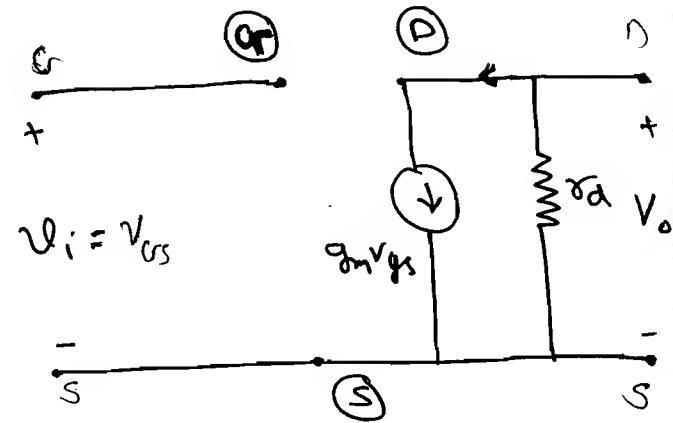
* Small signal equivalent ckt (or) AC equivalent
ckt.

⇒

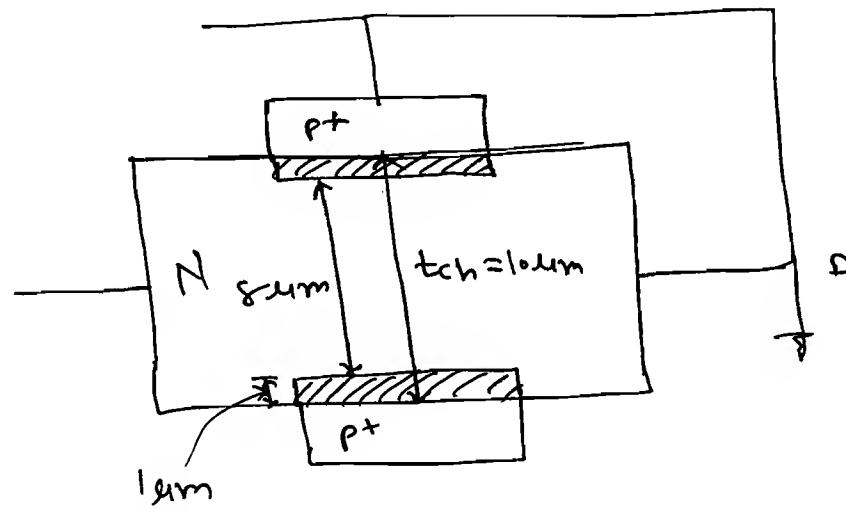
G •
+
 V_{GS}



$$= V_i = V_{GS}$$



[a]



$$V_{bi} = -1V.$$

fixed Channel resistance when $V_{GS} = 0V.$

$$R_{ch} = 600 \Omega \quad \text{when } t_{ch} = 10 \mu m.$$

$$R_{ch} = ? \quad \text{when } t_{ch} = 8 \mu m.$$

$$R_{ch} = \frac{SL}{W \times t_{ch}}.$$

Sum:

$$R_{ch1} = \frac{SL}{W \times t_{ch1}}, \quad R_{ch2} = \frac{SL}{W \times t_{ch2}}.$$

$$\therefore \frac{R_{ch_1}}{R_{ch_2}} = \frac{t_{ch_2}}{t_{ch_1}}.$$

$$\therefore R_{ch_2} = \frac{t_{ch_1}}{t_{ch_2}} \times R_{ch_1}$$

$$= \frac{10}{8} \times 600$$

$$R_{ch_2} = 750 \Omega$$

(Q-10) The Channel Resistance when $V_{GSS} = -3V$.

Soln: $V_J = \frac{eN_0}{2\epsilon} \cdot \omega^2$ ✓

$$\therefore V_J \propto \omega^2$$

$$\text{when } V_{GSS} = 0, \quad V_J = V_0 = -1V. = V_{bi}$$

$$\text{when } V_{GSS} = -3, \quad V_J = V_0 + V_F = -1 - 3 = -4V.$$

$$\omega = 14\text{m} \quad \text{when } V_{GSS} = 0.$$

$$\therefore \frac{V_{J1}}{V_{J2}} = \left(\frac{\omega_1}{\omega_2} \right)^2$$

$$\therefore \frac{t_{ch_1}}{t_{ch_2}} \propto \omega_2^2 = \frac{V_{J2}}{V_{J1}} \times \omega_1^2$$

$$\therefore \omega_2^2 = \frac{-4}{-1} \times (14\text{m})^2$$

$$\therefore \omega_2 = 28\text{m}$$

$$\therefore \text{Now, } t_{ch_3} = 10^{-2-2} = 6\text{m.}$$

$$\frac{R_{ch_3}}{R_{ch_1}} = \frac{t_{ch_1}}{t_{ch_3}}$$

$$\therefore R_{ch_3} = \frac{10}{6} \times 600$$

$$R_{ch_3} = 1000 \Omega$$

22) $\Rightarrow \underline{\text{FET}}$:

$$T \uparrow \rightarrow I_D \downarrow \quad P_D = V_{SD} \cdot I_D$$

NTC

\Rightarrow FET is very much stable than BJT as it has -ve temp. coefficient.

* Biassing techniques

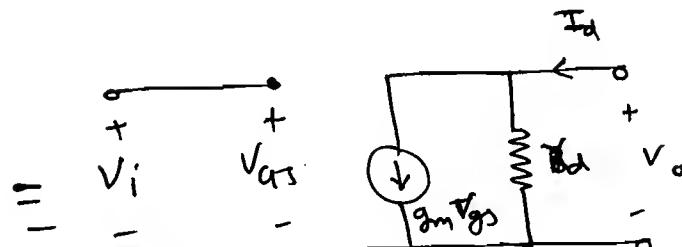
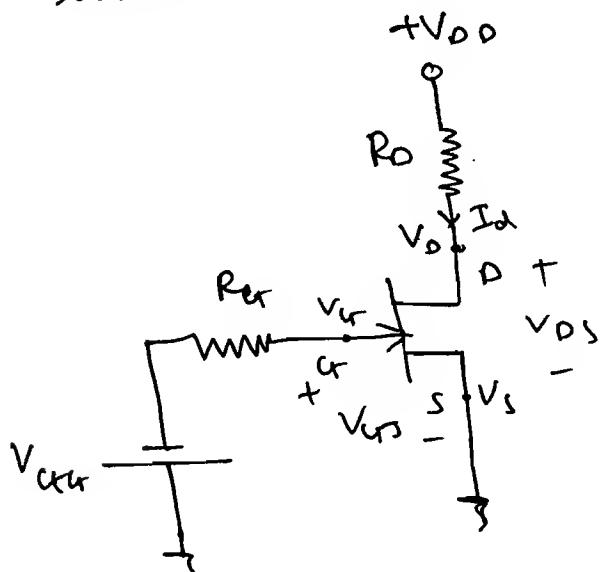
For JFET: [dc analysis]

① Fixed biassed.

② Self biassed.

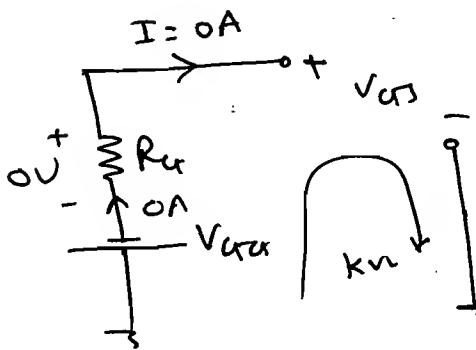
③ Voltage divider biassed.

① Fixed biassed:

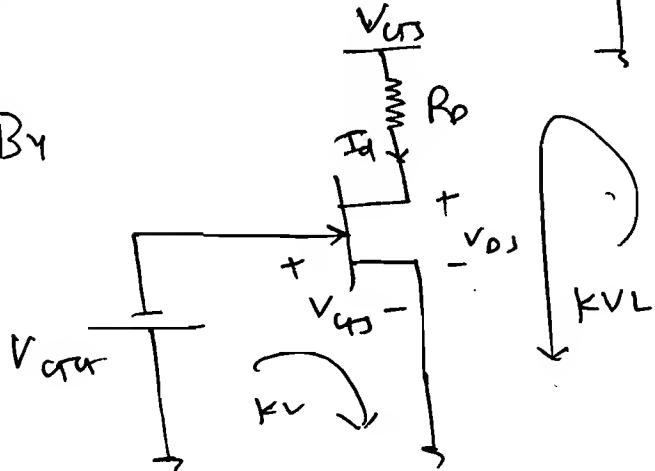


$$\Rightarrow V_{DS} = V_D - V_S$$

$$V_{GDS} = V_G - V_S$$



$\Rightarrow B_V$



$$\Rightarrow \text{By KVL} \quad -V_{act} - V_{crs} = 0.$$

$$\therefore V_{AB} = -V_{AA} \quad \square$$

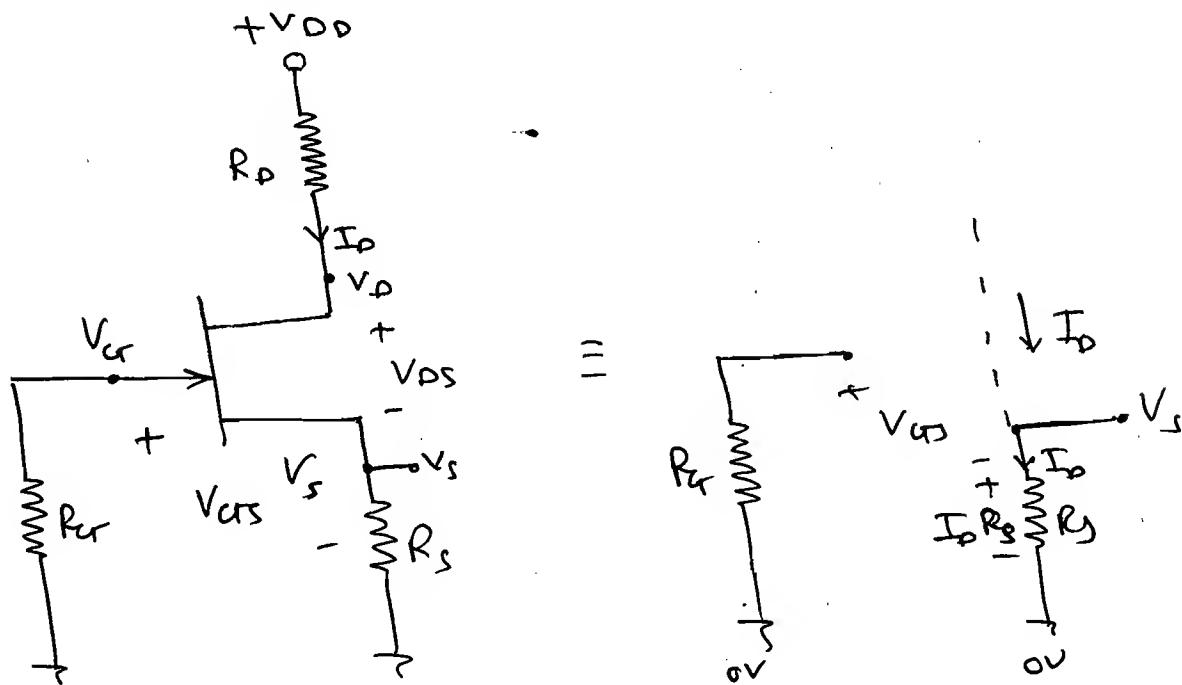
$$\Rightarrow I_0 = I_{oss} \left[1 - \frac{V_{oss}}{V_p} \right]^2$$

$$\therefore I_o = I_{oss} \left[1 + \frac{V_{aer}}{V_p} \right]^2. \quad \checkmark$$

$$\Rightarrow B_4 kn, \\ V_{DD} - I_D R_o - V_{DS} = 0.$$

$$V_{DS} = V_{DD} - I_{DS} R_D$$

② Self - biased :



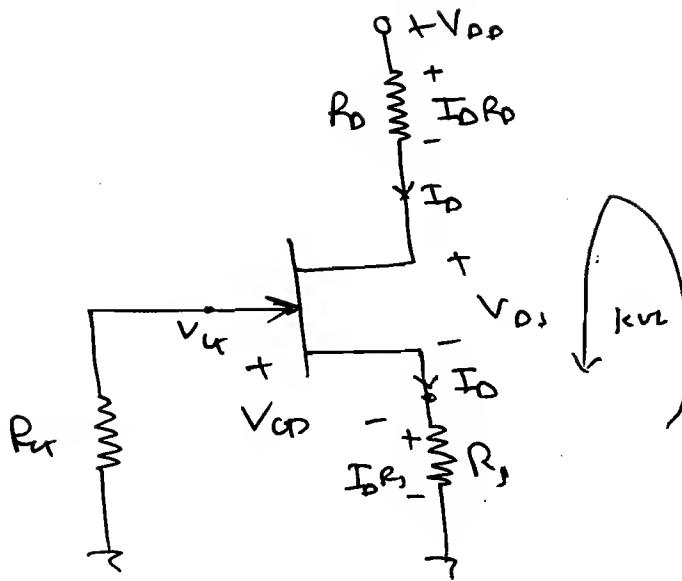
$$\Rightarrow V_{ws} = V_C - V_S$$

$$B_y, \text{ kV/m} \quad 0 - V_{AS} - I_B R_S = 0$$

$$V_{DS} = V_D - V_S.$$

$$\Rightarrow V_{UR_3} = -I_0 R_3.$$

\Rightarrow



$$\Rightarrow B_u, k_{VL}, V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0.$$

$$\therefore V_{DS} = V_{DD} - I_D (R_D + R_S).$$

$$\text{But, } I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

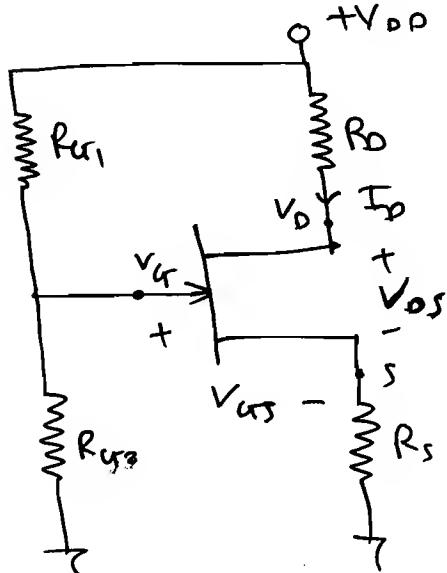
$$V_{GS} = -I_D \cdot R_G$$

$$\therefore I_D = I_{DSS} \left[1 + \frac{I_D R_G}{V_P} \right]^2$$

$$\therefore V_{DS} = V_{DD} - I_{DSS} \left[1 + \frac{I_D R_G}{V_P} \right]^2 \cdot (R_D + R_S)$$

③

Voltage - Divider biased:

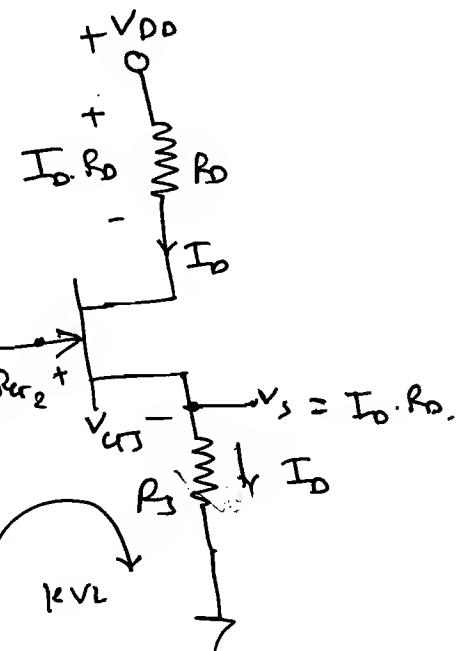


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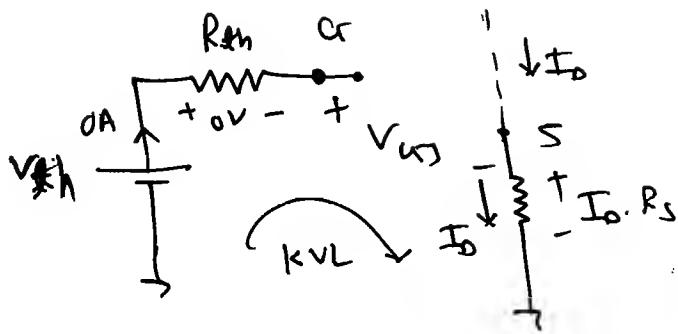
$$V_{CR} = \frac{R_{CR} V_{DD}}{R_{CR} + R_{CR}}$$

$$= R_{CR} \parallel R_{CR} + R_{CR}$$

$$= R_{CR} \parallel R_{CR}$$



$$\Rightarrow V_{GSS} = V_G - V_S$$



$$\Rightarrow V_G = V_{TH} + 0$$

$$V_G = V_{TH}.$$

$$V_G - V_{GSS} - I_D \cdot R_S = 0.$$

$$\boxed{V_{GSS} = V_G - I_D \cdot R_S.}$$

$$V_G = V_{TH} = \frac{R_{G2}}{R_{G1} + R_{G2}} \times V_{DD}.$$

$$\Rightarrow I_D = I_{DSS} \left[1 - \frac{V_{GSS}}{V_P} \right]^2.$$

$$\therefore \boxed{I_D = I_{DSS} \left[1 - \frac{V_G - I_D \cdot R_S}{V_P} \right]^2.}$$

$$\Rightarrow V_{DD} = I_D \cdot R_D + V_{DS} + I_D \cdot R_S.$$

$$\therefore \boxed{V_{DS} = V_{DD} - I_D (R_D + R_S).} \quad \checkmark$$

Now, V_{GSS} should be $-ve.$

$$\text{So, } I_D \cdot R_S > V_G.$$

$$\frac{V_{DS} - V_{DD}}{R_D + R_S} \cdot R_S > V_G$$

Select R_D & R_S in a such a way

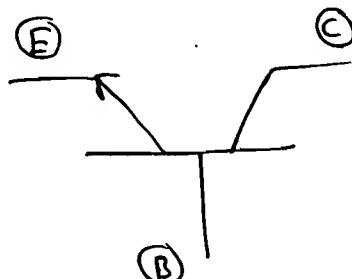
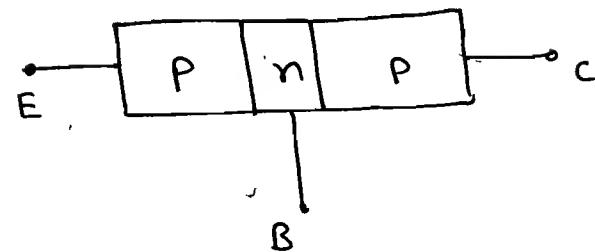
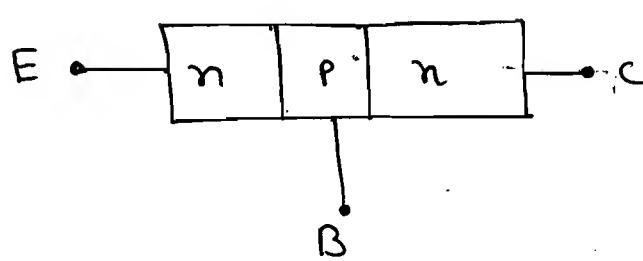
$$\text{that } I_D \cdot R_S > V_G \Rightarrow V_{GSS} = -ve.$$

Amplifier

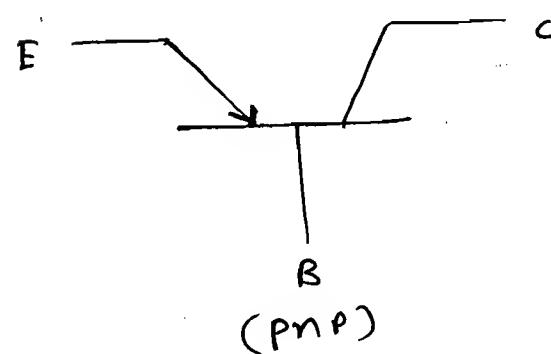
Analysis: (AC Analysis):

24)

⇒



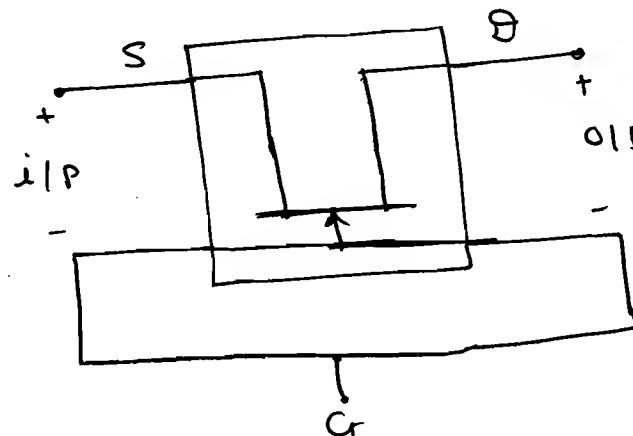
(n-p-n)



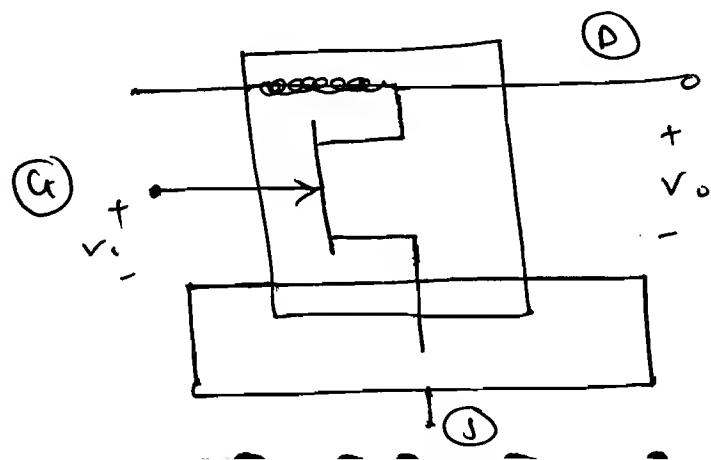
(p-n-p)

⇒ Configuration or JFET:

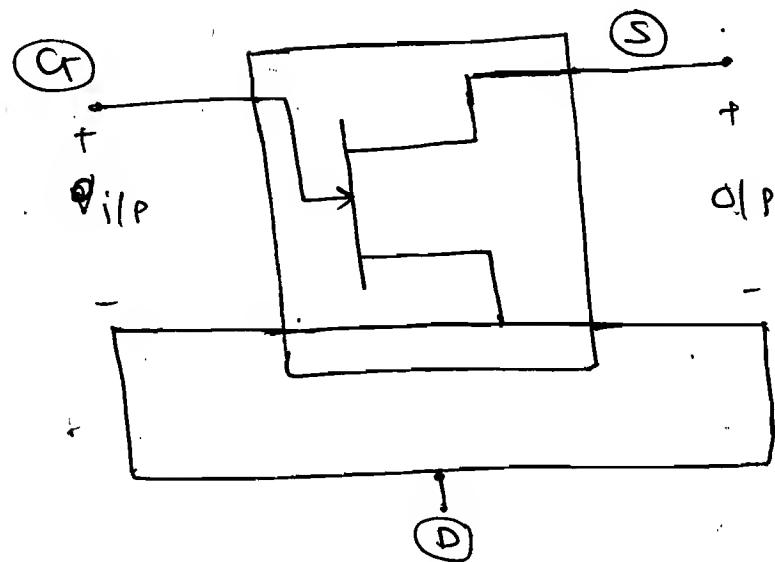
① Common gate Configuration:



② Common source Configuration:



3 Common Drain Configuration:



(Source follower)

Note:

⇒ CD and CS can not be used as the current amplifiers because FET has high input impedance and O/P impedance. i.e. at input it is open ckt. Therefore no input current. As in CD and CS input ~~is~~ is given to the gate and when ~~is~~ ^{the} i/p is given to gate it is open ckt. and they can be used as current amplifiers. In common gate $I_D = I_S$ so, current gain is 1. i.e. no amplification.

$$A_{i/o} = \frac{I_o}{I_i} = \frac{I_o}{I_f} = 1.$$

No current amplification.

①

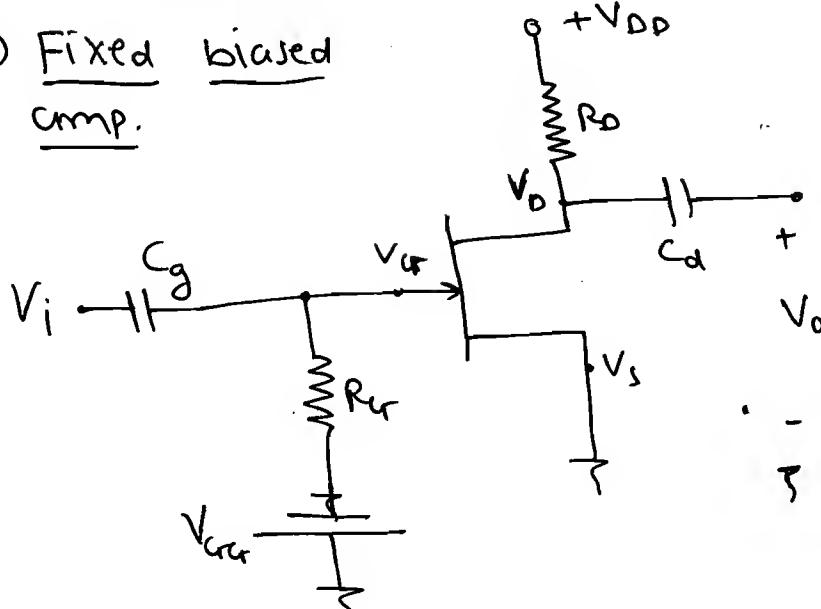
Common

Source

Configuration

Ampifier. 25)

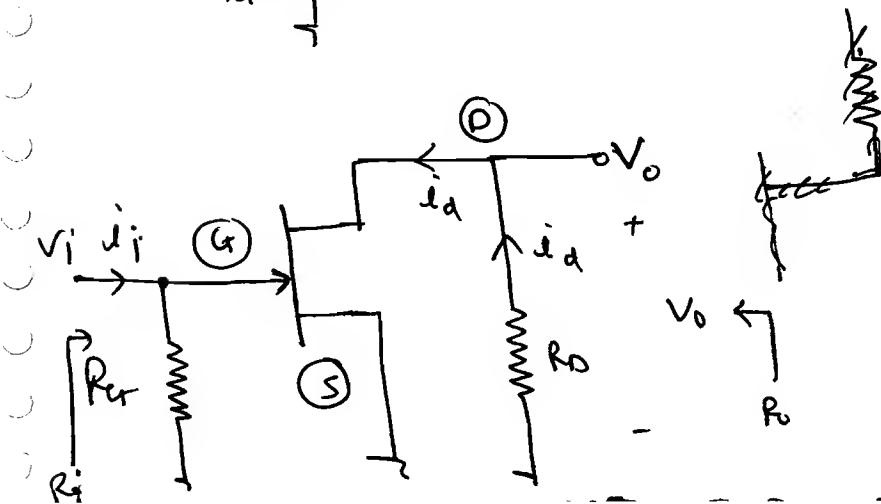
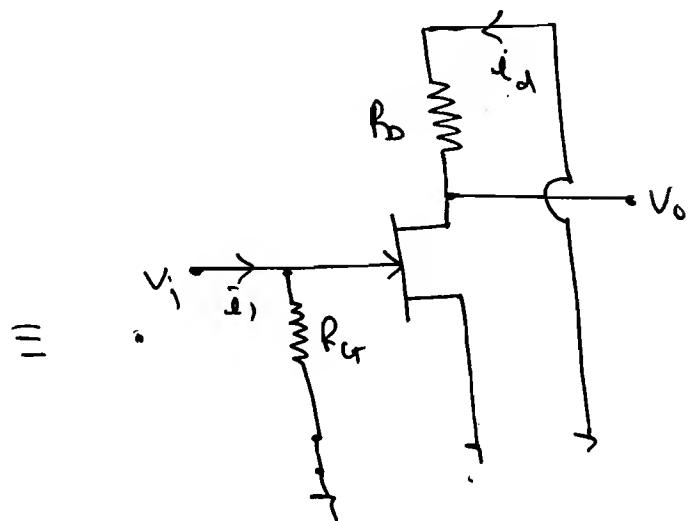
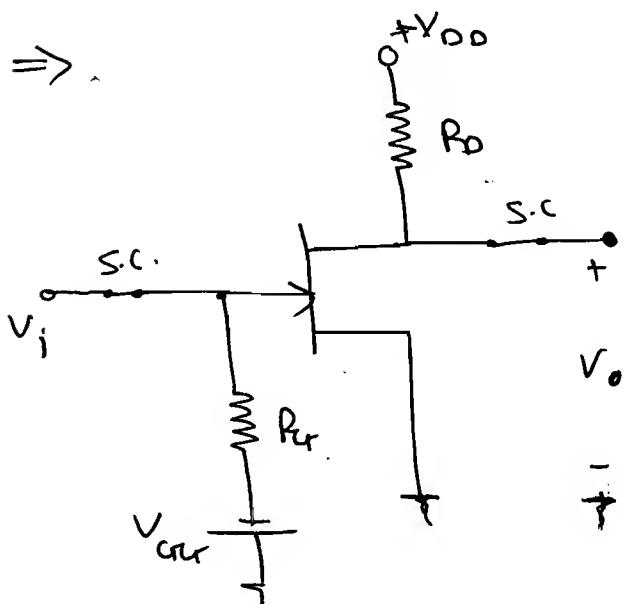
(1.) Fixed biased
Cmp.



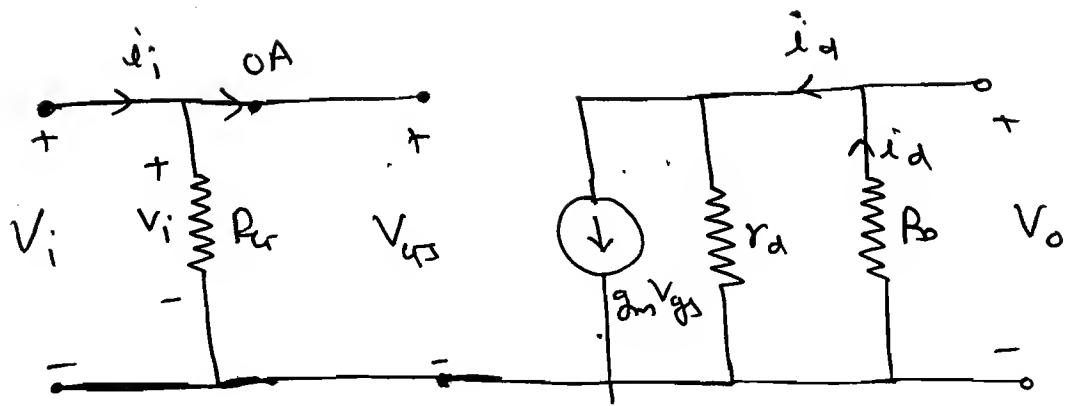
Steps:

- ① Short Ckt the Capacitance.
- ② Short Ckt the d.c. power supply to Ground.
- ③ Identify the terminals of JFET.
- ④ Replace JFET with its eqⁿ Ckt.

⇒



Eqn Ckt:



Small signal eqn Ckt (or)
 h-parameter eqn Ckt (or)
 AC eqn Ckt.

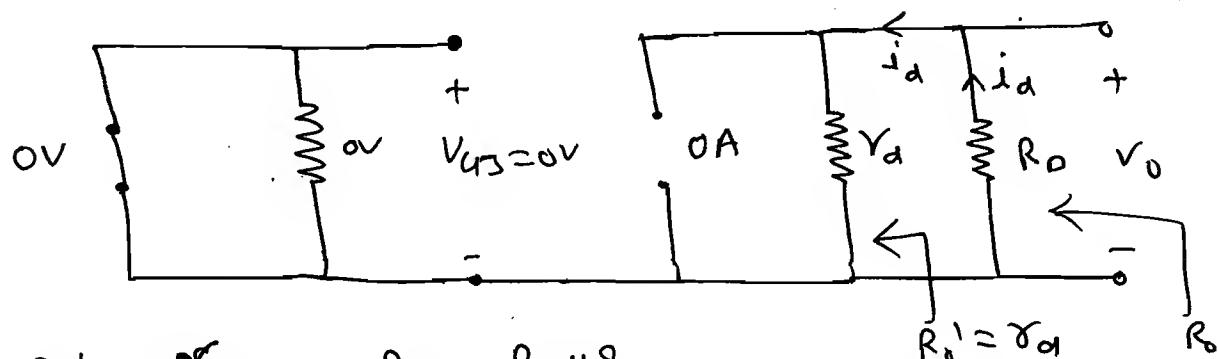
① Input Resistance (R_i):

$$\Rightarrow \text{input resistance } R_i = \frac{2i_i}{i_i} = \frac{2i_i \cdot R_{cr}}{i_i} = R_{cr}.$$

$$\therefore R_i = R_{cr}$$

② Output Resistance (R_o):

\Rightarrow for finding R_o make d.c. = 0.



$$\Rightarrow R_o' = \gamma_d, \quad R_o = R_d \parallel \gamma_d.$$

$$\therefore R_o = \gamma_d \parallel R_o.$$

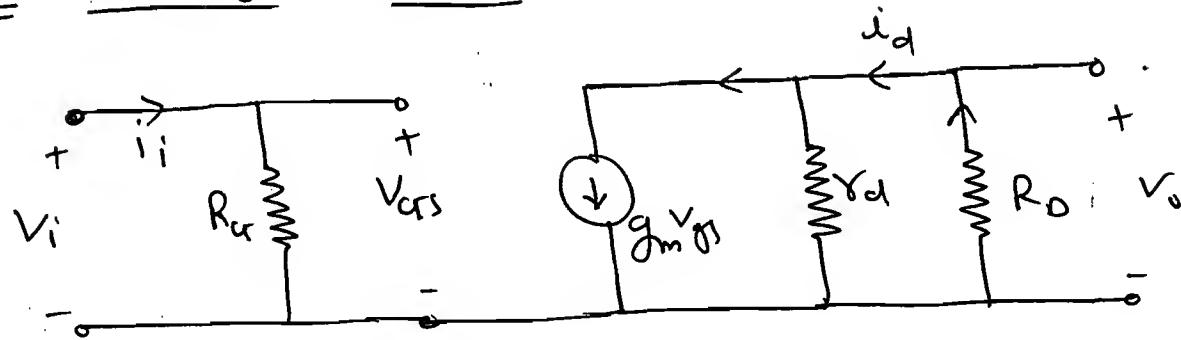
ideally $\gamma_d = \infty$.

practically $\gamma_d = 50k$ to $100k$

26)
So, for $r_d \gg R_o$. (or) $r_d \geq 10R_o$.

$$R_o \approx R_d.$$

③ Voltage gain:



$$\therefore V_i = R_g \cdot i_i = V_{gs}.$$

$$\therefore V_o = -g_m V_{gs} \cdot [r_d \parallel R_o].$$

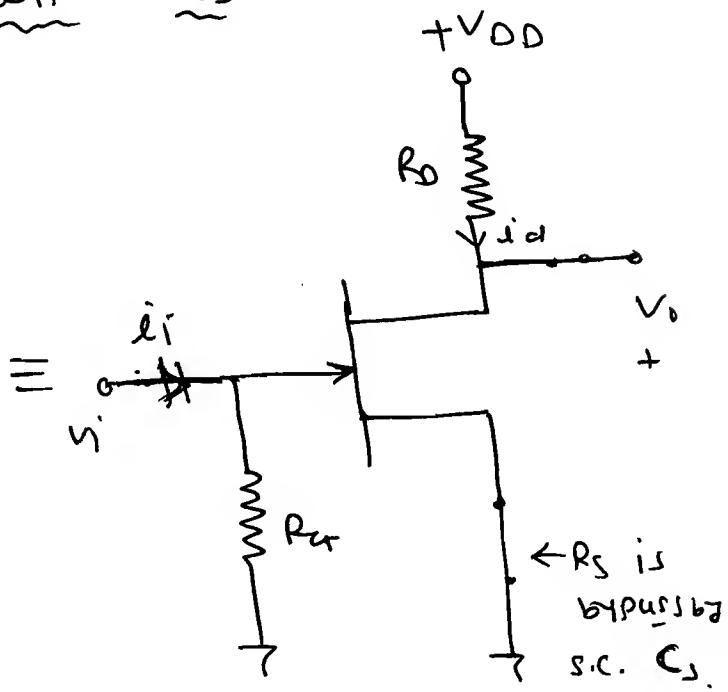
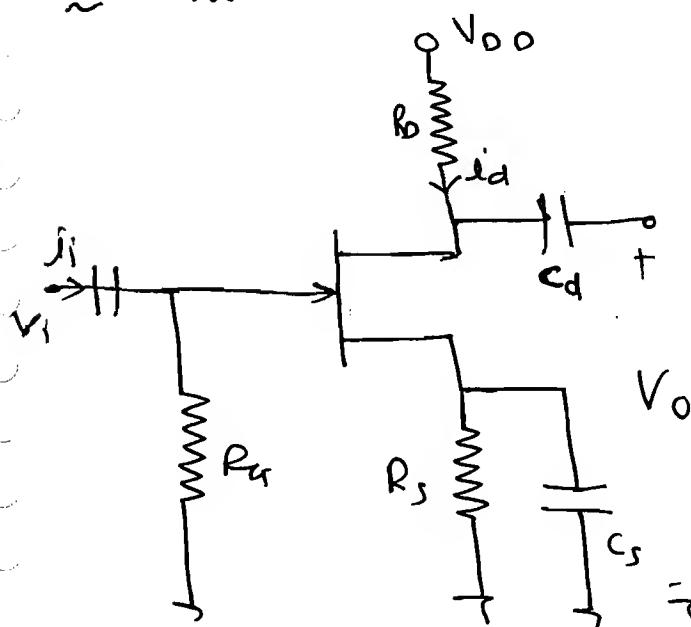
$$\therefore A_v = \frac{V_o}{V_i} = -\frac{g_m V_{gs} [r_d \parallel R_o]}{V_{gs}}$$

$$\therefore A_v = -g_m [r_d \parallel R_o].$$

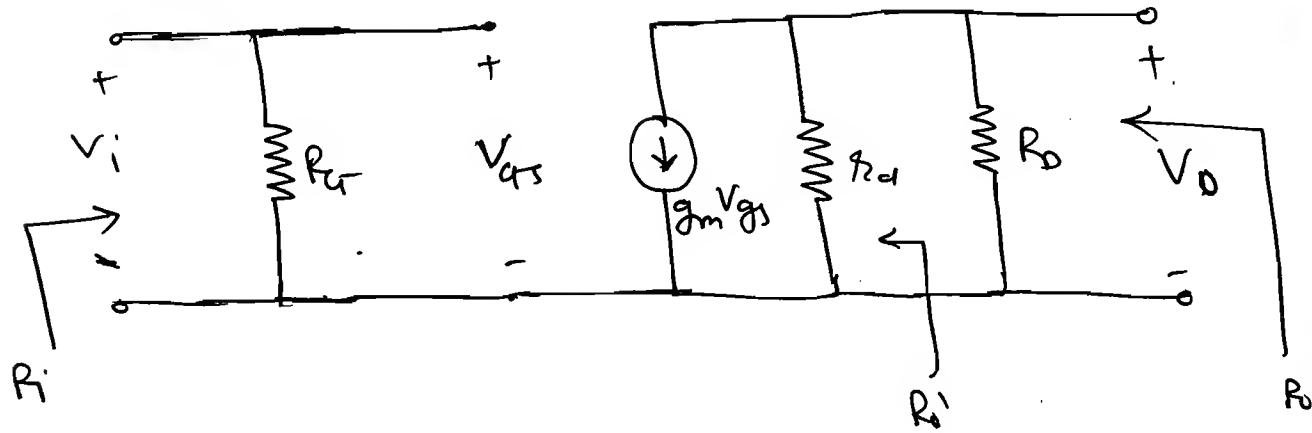
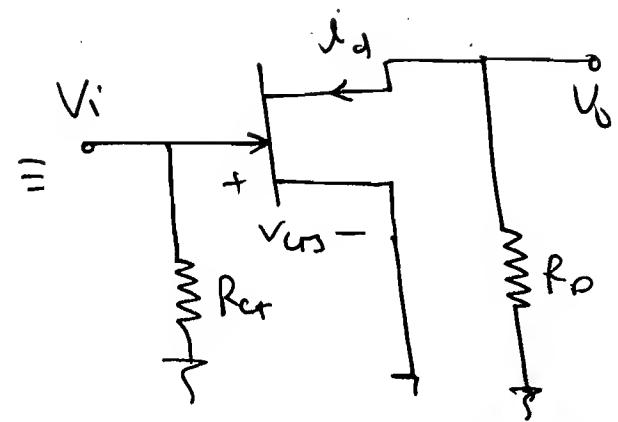
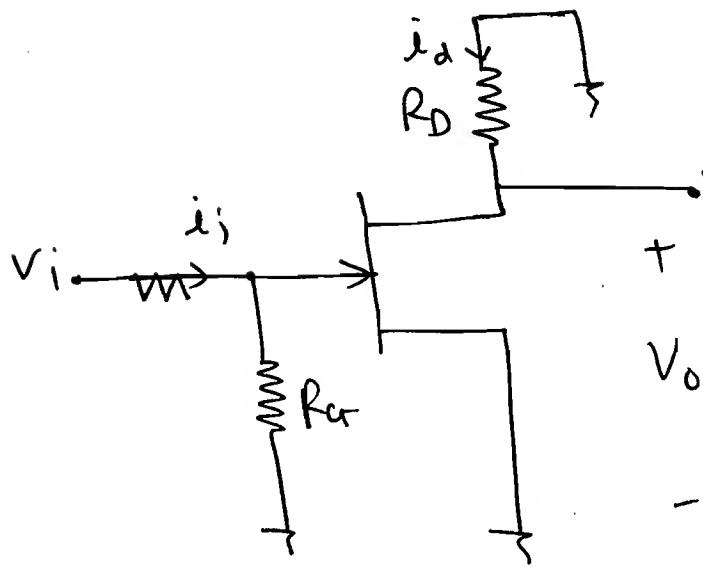
$$\text{But } r_d \gg R_o \Rightarrow r_d \parallel R_o \approx R_o.$$

$$\therefore A_v = -g_m R_o.$$

② Self bias cmp. (with C_s):



\Rightarrow



① Input Resistance:

\Rightarrow Input Resistance

$$R_i = R_G$$

② Output Resistance:

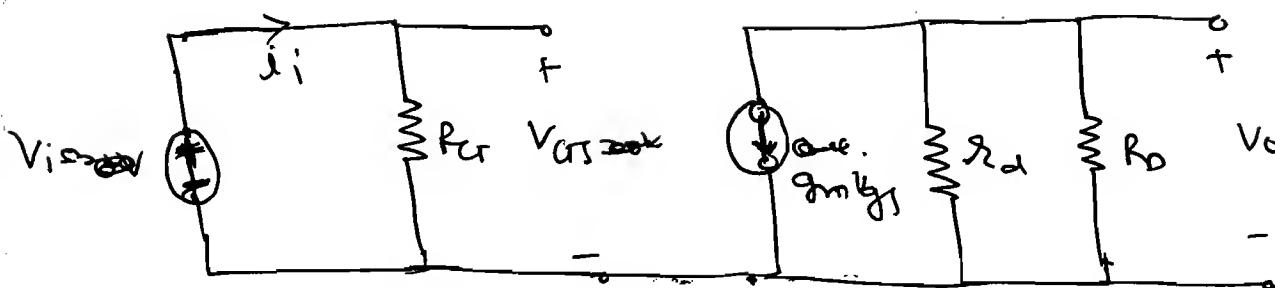
$$\Rightarrow R_o' = R_D, \quad R_o = R_D \parallel R_o'$$

$$\therefore R_o = R_D \parallel R_o'$$

$$\therefore R_o \approx R_D \quad (\because R_D \gg R_o).$$

③ Voltage gain:

277



$$V_{GS1} = V_i$$

$$\therefore V_o = -g_m V_{GS1} [R_d \parallel R_o]$$

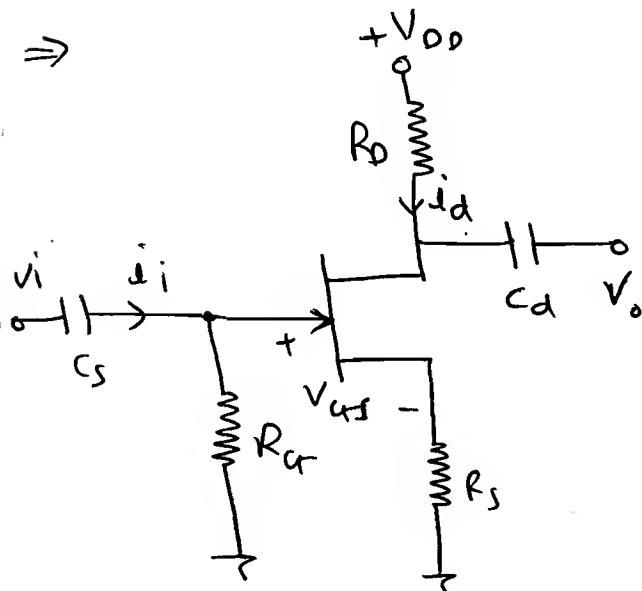
$$\therefore A_v = \frac{V_o}{V_i} = -\frac{g_m V_{GS1} [R_d \parallel R_o]}{V_{GS1}}$$

$$A_v = -g_m [R_d \parallel R_o]$$

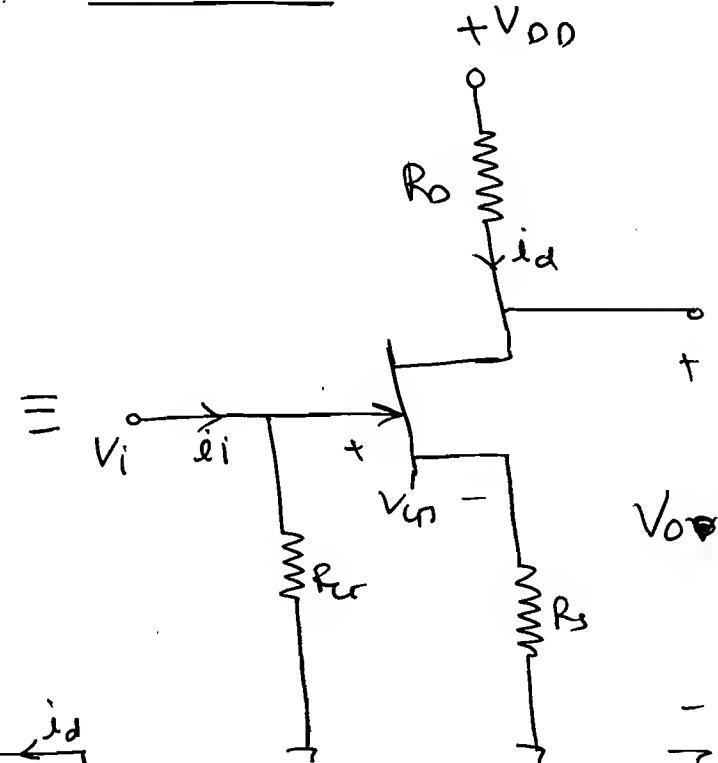
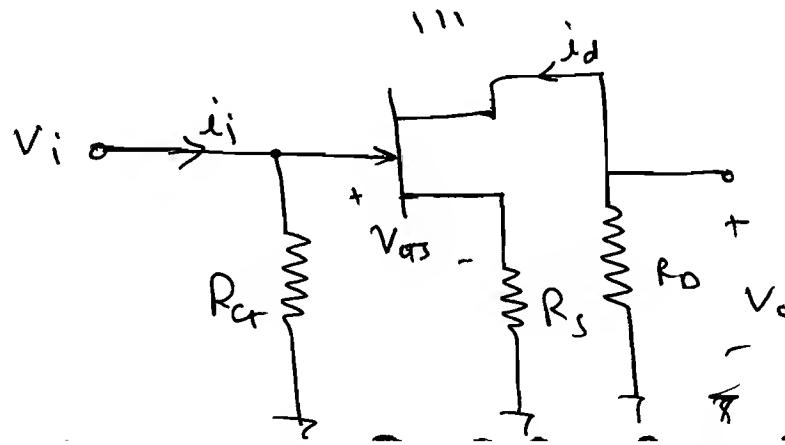
$$A_v \approx -g_m R_o \quad (\because R_d \gg R_o)$$

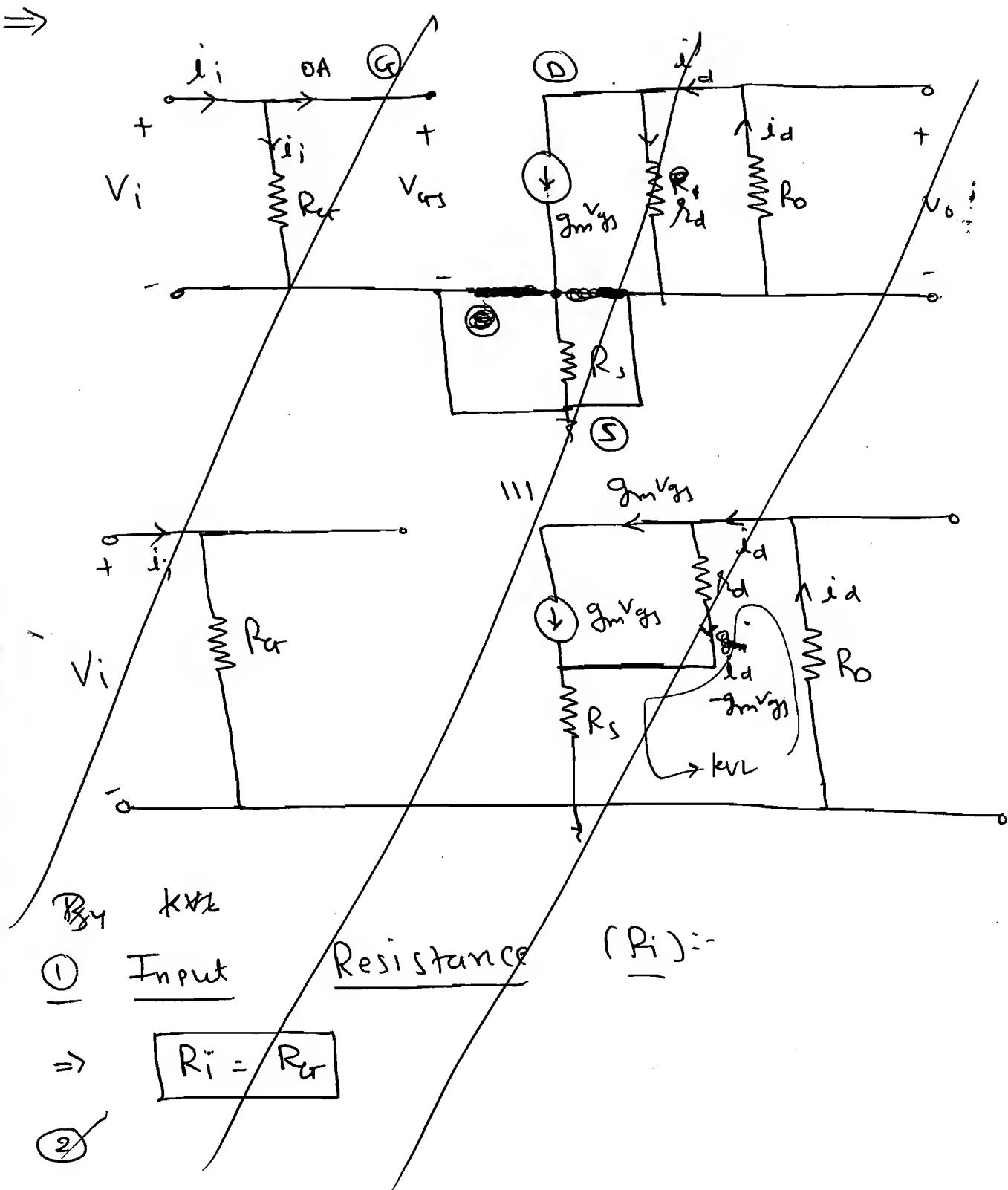
③ Self biassed amp. (without C_s):

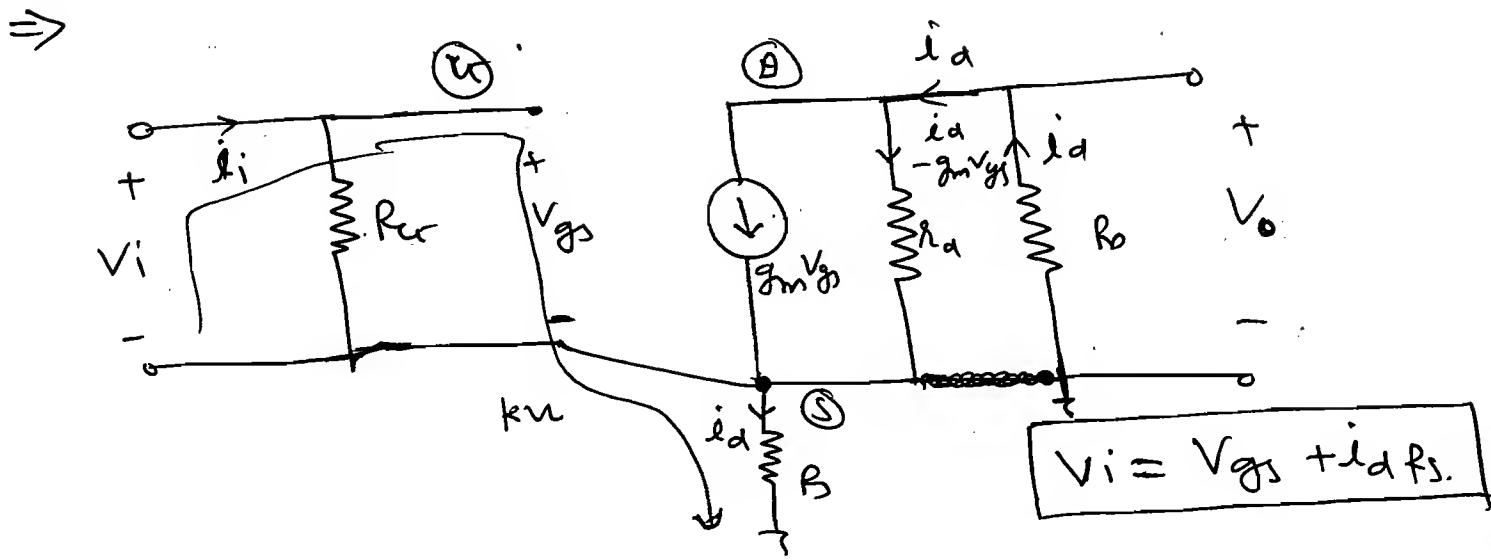
\Rightarrow



\Rightarrow



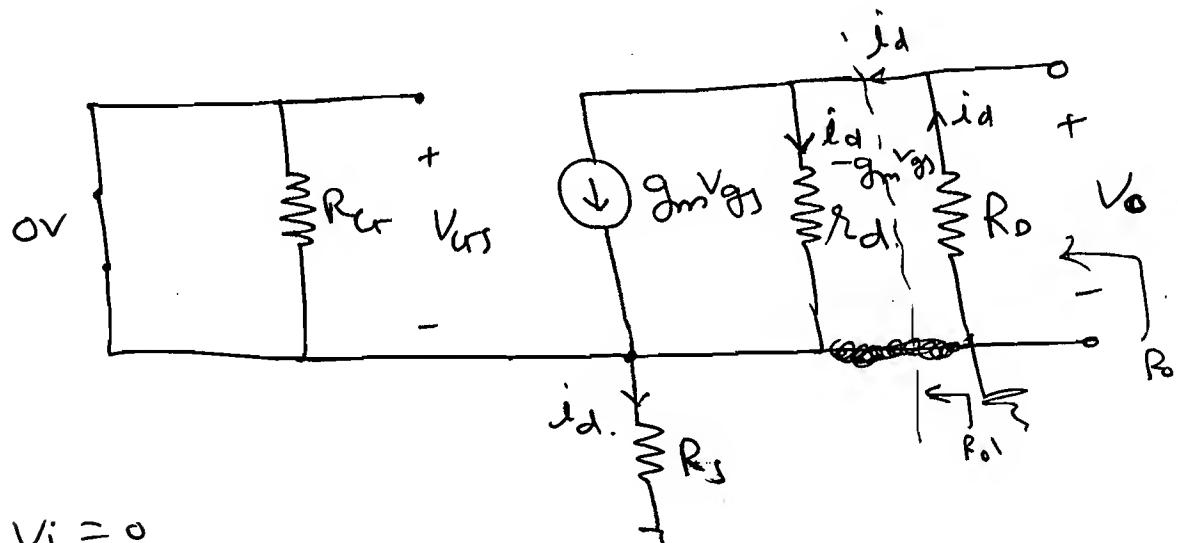




① Input Resistance (R_i):

$$\Rightarrow \text{Input Resistance} \quad R_i = R_{in}$$

② Output Resistance (R_o):



as $Vi = 0$

$$\Rightarrow V_{o1} = -id \cdot R_s.$$

$$\text{By Kirchhoff's Law, } V_o = \eta_d (id - g_m V_{gs}) + R_s \cdot id.$$

$$\therefore R_o = R_D \parallel R_s$$

$$R_o' = \frac{2\eta_d}{id}$$

$$\eta_d (1 + g_m \eta_d) + R_s$$

$$\therefore \frac{V_o}{id} = R_o' = \eta_d + (1 + g_m \eta_d) R_s.$$

$$R_o = R_o \parallel [R_d + (1+u)R_s]$$

($\because u = g_m r_d$).

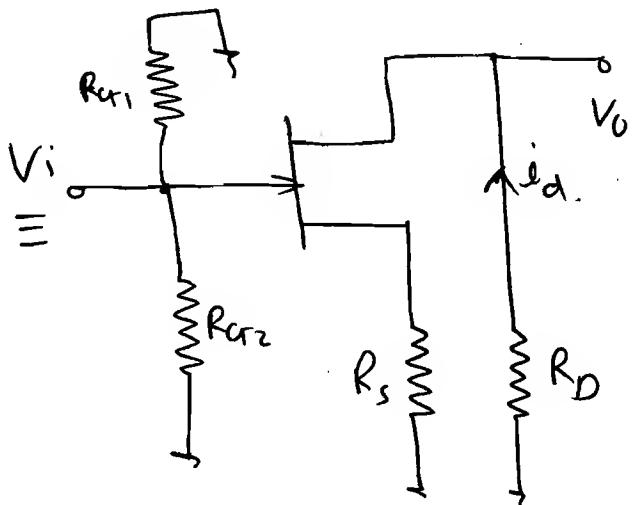
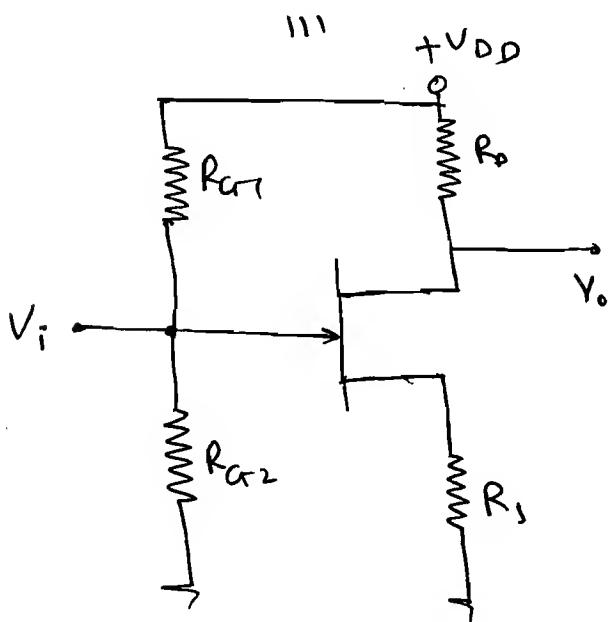
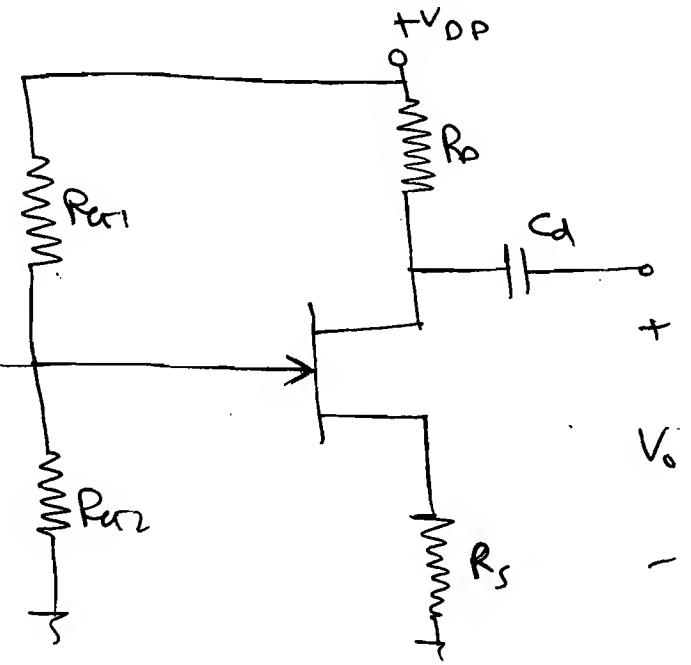
③ Voltage gain: (A_v) :

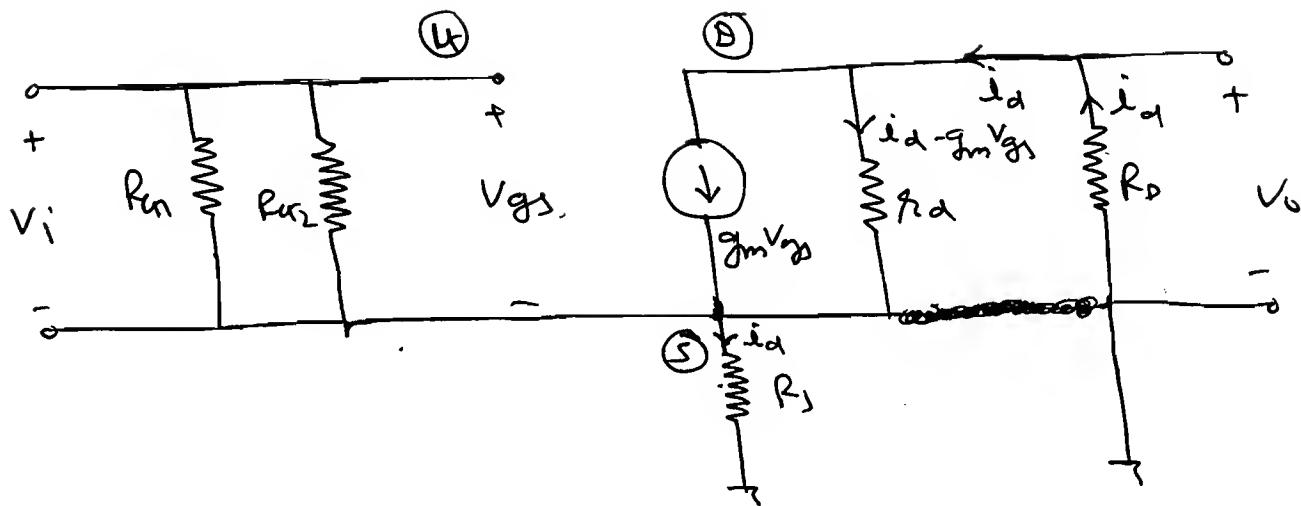
$$V_i = V_{gs} + i_d R_s$$

$$V_{gs} = V_i - i_d R_s$$

$$A_v = \frac{-g_m R_o}{1 + g_m R_s}$$

④ Voltage - divider bias amp (without C_s):





① Input Resistance (R_i):

$$\Rightarrow R_i = R_{g1} \parallel R_{g2}$$

② Output Resistance (R_o):

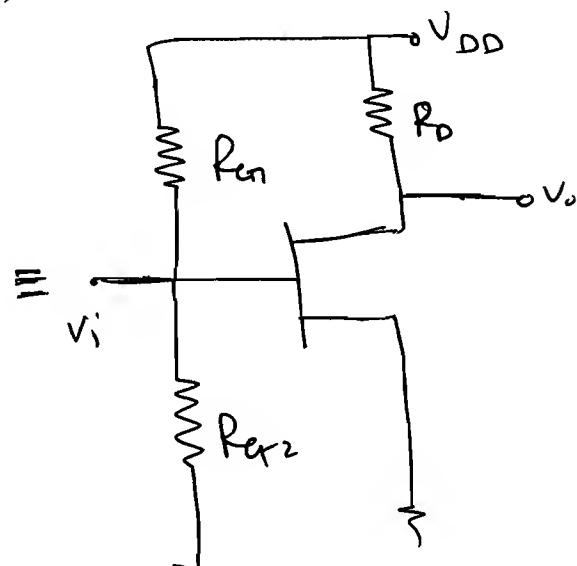
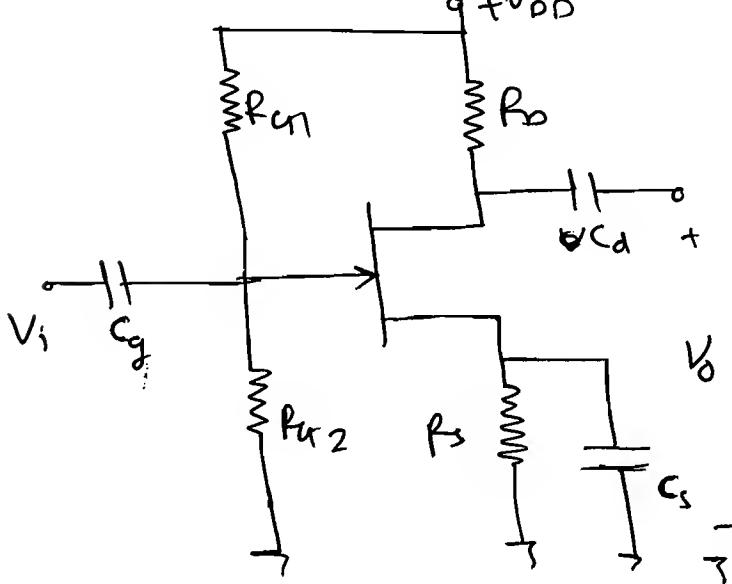
$$\Rightarrow R_o = R_D \parallel [r_d + (1 + \mu) R_s].$$

($\because \mu = g_m r_d$).

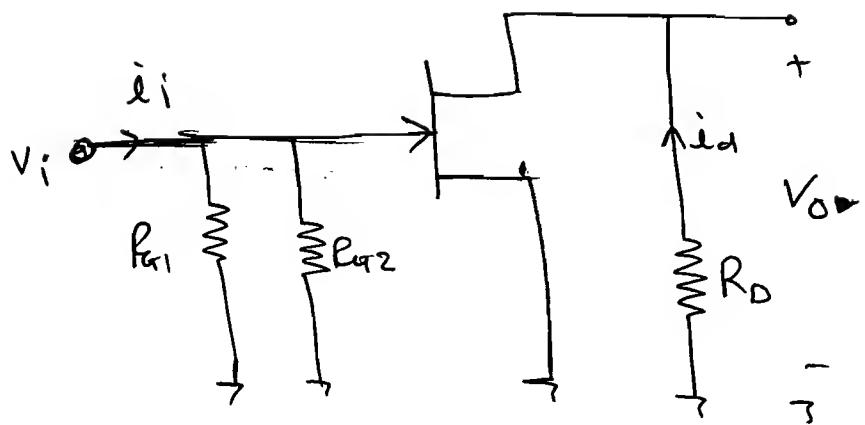
③ Voltage gain: (A_v):

$$\Rightarrow A_v = \frac{-g_m R_o}{1 + g_m R_s}$$

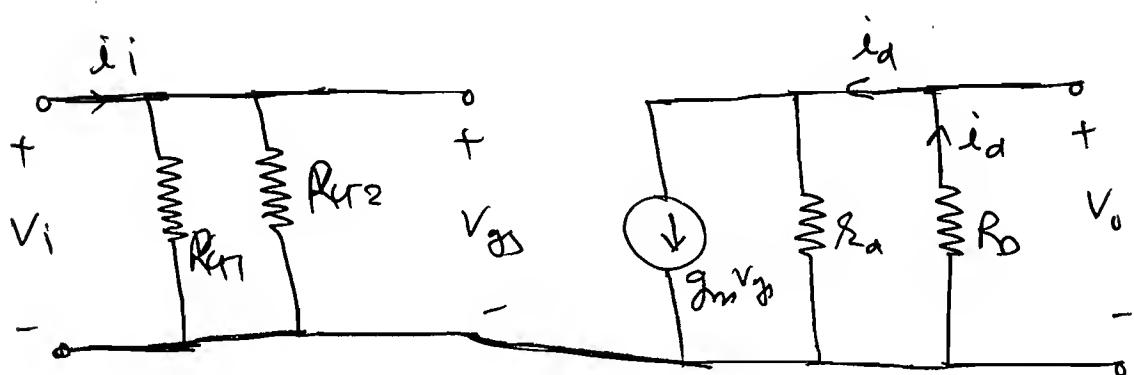
④ Voltage divider bias (with C_s):



⇒



III



① Input Resistance:

$$\Rightarrow R_i = R_{g1} \parallel R_{g2}.$$

② Output Resistance (Ro):

$$\Rightarrow R_o = R_D \parallel R_d \approx R_D \quad (\because R_d \gg R_D).$$

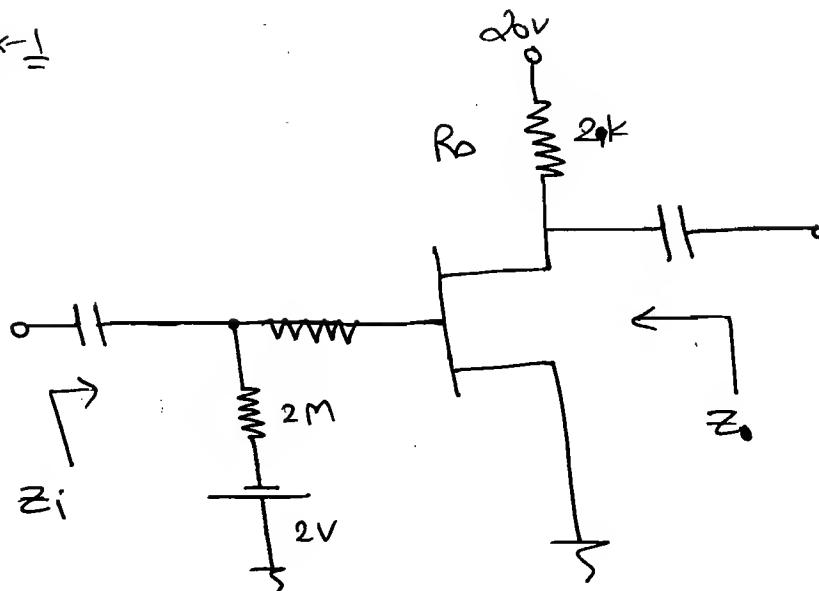
③ Voltage gain (Av):

$$\Rightarrow A_v = -g_m \cdot (R_o \parallel R_d)$$

$$\therefore A_v = -g_m \cdot R_o.$$

Ex-1

30)



$$R_D = 20k$$

$$I_{DSS} = 10mA$$

$$V_P = -8V$$

$$\text{Q-10} \quad z_i = R_i = 2M \Omega$$

$$z_o = R_D \parallel R_D = \frac{2k}{20k} \parallel 20k = \frac{40}{22} = \frac{20}{11} k\Omega$$

Q-11

$$I_D = I_{DSS} \left[1 - \frac{-V_{GS}}{V_P} \right]^2$$

$$I_D = 10mA \left[1 - \frac{-2}{-8} \right]^2 \quad \left| \begin{array}{l} V_{DS} = V_{DD} - I_D R_D \\ = 20V - 5.625mA \times 2k \end{array} \right.$$

$$\boxed{I_D = 5.625mA}$$

$$V_{DS} = 8.75V$$

Q-12

$$g_m = \left| \frac{2I_{DSS}}{-V_P} \right| \cdot \left[1 - \frac{V_{GS}}{V_P} \right]$$

$$\therefore g_m = \frac{2 \times 10mA}{8} \times \left[1 - \frac{-2}{-8} \right]$$

$$\therefore \boxed{g_m = 1.875 \text{ mA/V.}}$$

Q-13

$$A_V = -g_m (R_D \parallel R_D)$$

$$A_V = -1.875 \text{ mA} \left(\frac{20k}{11} \right)$$

$$\boxed{A_V = -3.4}$$

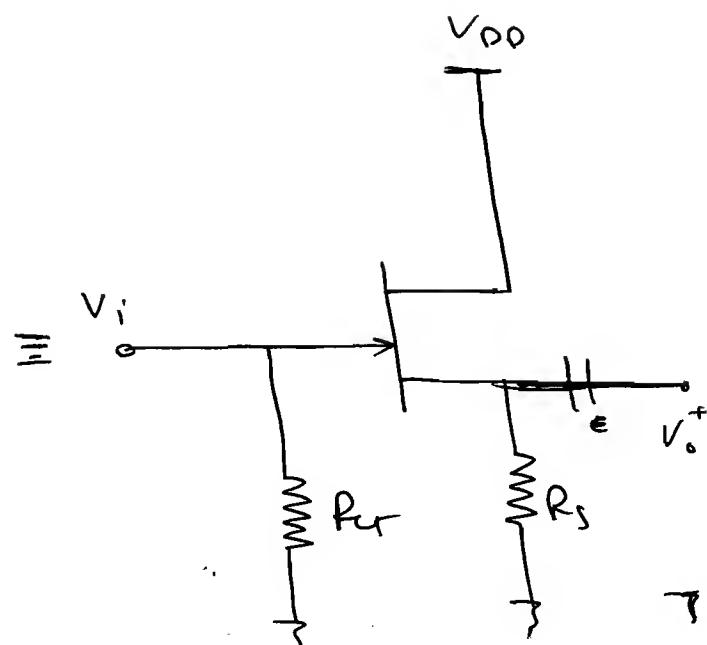
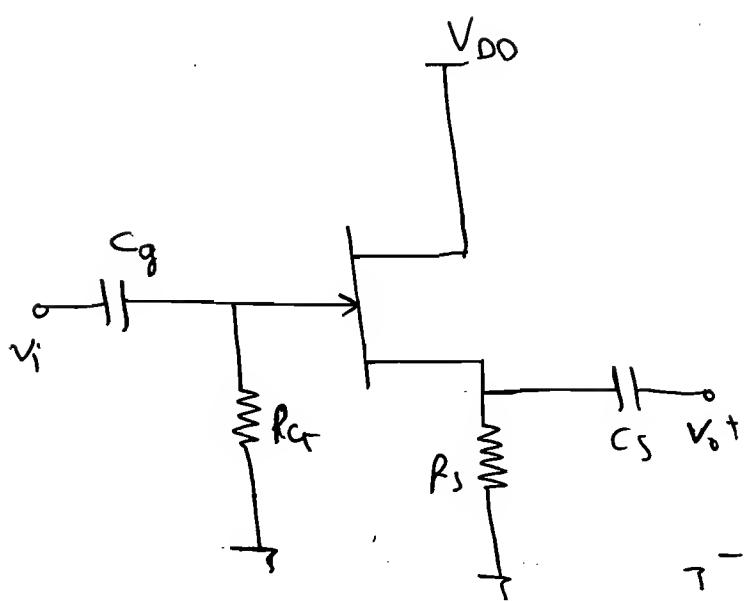
Parameters	Fixed bias amp	Self bias amp	Voltage dividers amp.
1. R_i	$R_i = R_a$	$R_i = R_{a1}$	$R_i = R_{a1} \parallel R_{a2}$
2. R_o	$R_o = R_{o1} \parallel R_{a2}$ $R_o \approx R_o$	$R_o = R_{o1} \parallel R_{a2}$ $R_o \approx R_o$	$R_o = R_{o1} \parallel R_{o2}$ $R_o \approx R_o$
3. A_V	$-g_m (R_{o1} \parallel R_{a2})$ $= -g_m \cdot R_o$	$\frac{-g_m R_o}{1 + g_m R_s}$	$\frac{-g_m R_o}{1 + g_m R_s}$

② Common

Drain

Amplifier:

① Self bias:



$$\Rightarrow R_i = R_{DS}$$

$$R_o = r_d \parallel R_s \parallel \frac{1}{g_m}$$

if $r_d \gg R_s$

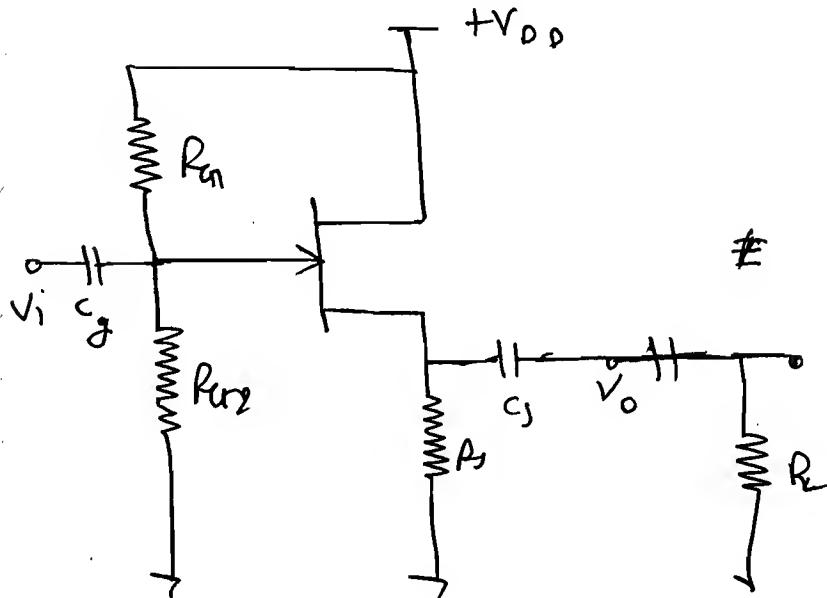
$$\therefore R_o = R_s \parallel \frac{1}{g_m}$$

$$V_o = \frac{g_m (r_d \parallel R_s)}{1 + g_m (r_d \parallel R_s)}$$

if $r_d \gg R_s$

$$V_o = \frac{g_m R_s}{1 + g_m R_s}$$

② Voltage divider:



$$\rightarrow R_i = R_{sr1} \parallel R_{sr2}$$

$$R_o = R_s \parallel \frac{1}{gm}$$

$$Av = \frac{gm \cdot R_s}{1 + gm \cdot R_s}$$

if R_L is connected,

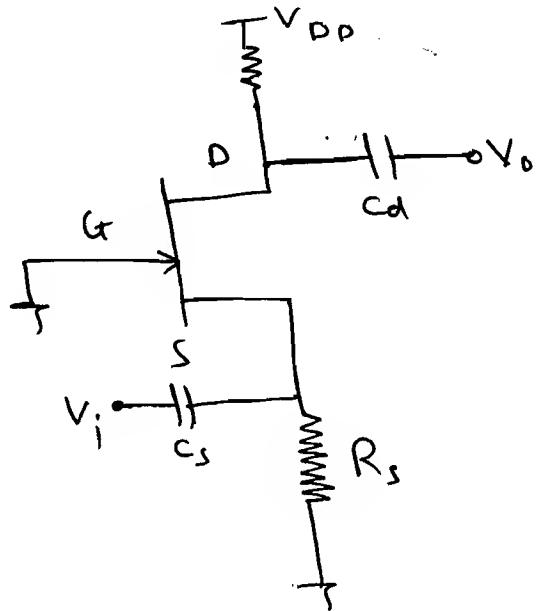
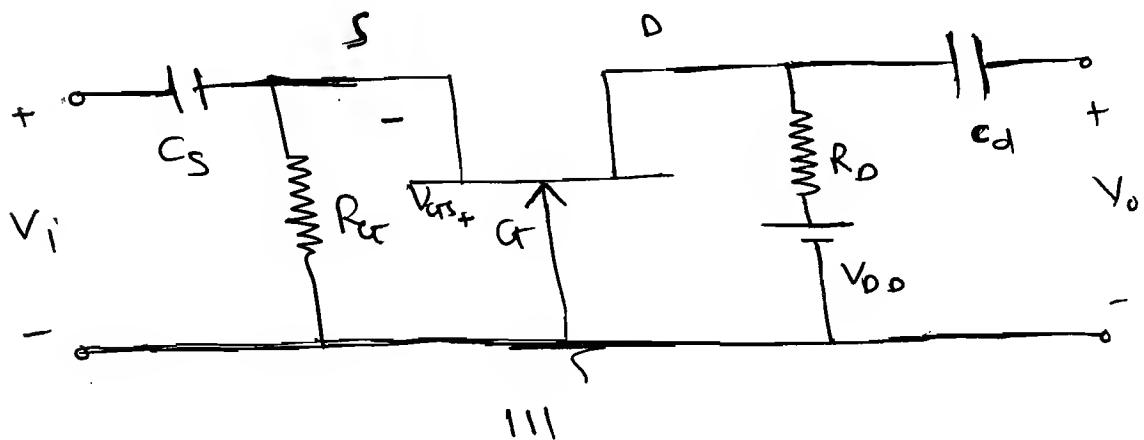
$$R_i = R_{sr1} \parallel R_{sr2}$$

$$R_o = R_s \parallel \frac{1}{gm} \parallel R_L$$

$$Av = \frac{gm \cdot (R_s \parallel R_L)}{1 + gm(R_s + R_L)}$$

③ Common gate Configuration Amp.

\Rightarrow



$$R_i \approx R_s \parallel \frac{1}{gm}$$

$$R_o = \frac{1}{gm} \parallel R_D$$

$$Av = gm \left(\frac{1}{gm} \parallel R_D \right)$$

if $\frac{1}{gm} \gg R_D$

$$R_o \approx R_D$$

$$Av \approx gm R_D$$

*

BJT

$$C_B = 0$$

$$C_E = 180^\circ$$

$$C_C = 0^\circ$$

FET

$$C_G = 0^\circ$$

$$C_S = 180^\circ$$

$$C_D = 0^\circ$$

① BJT:

	A_I	A_v
C_B :	≈ 1	High
C_E :	High	High
C_C :	High	≈ 1

Voltage gain	Current gain
$A_{vcc} \approx 1$	$A_{icb} \approx 1$
$A_{vcB} > A_{vce}$	$A_{icc} > A_{ice}$
$A_{cc} < A_{vce} < A_{vcB}$	$A_{icb} < A_{ice} < A_{icc}$

② FET:

Voltage gain

Current gain

$$C_D: A_{vD} = \frac{g_m R_s}{1 + g_m R_s} \approx 1$$

$$C_G: A_{icG} = \frac{I_o}{I_s} = 1$$

$$C_S: A_{vCs} \quad \left. \begin{array}{l} A_{vcr} > A_{vcs} \\ C_G = A_{vcr} \end{array} \right\}$$

$$A_{vco} < A_{vcs} < A_{vcr}$$

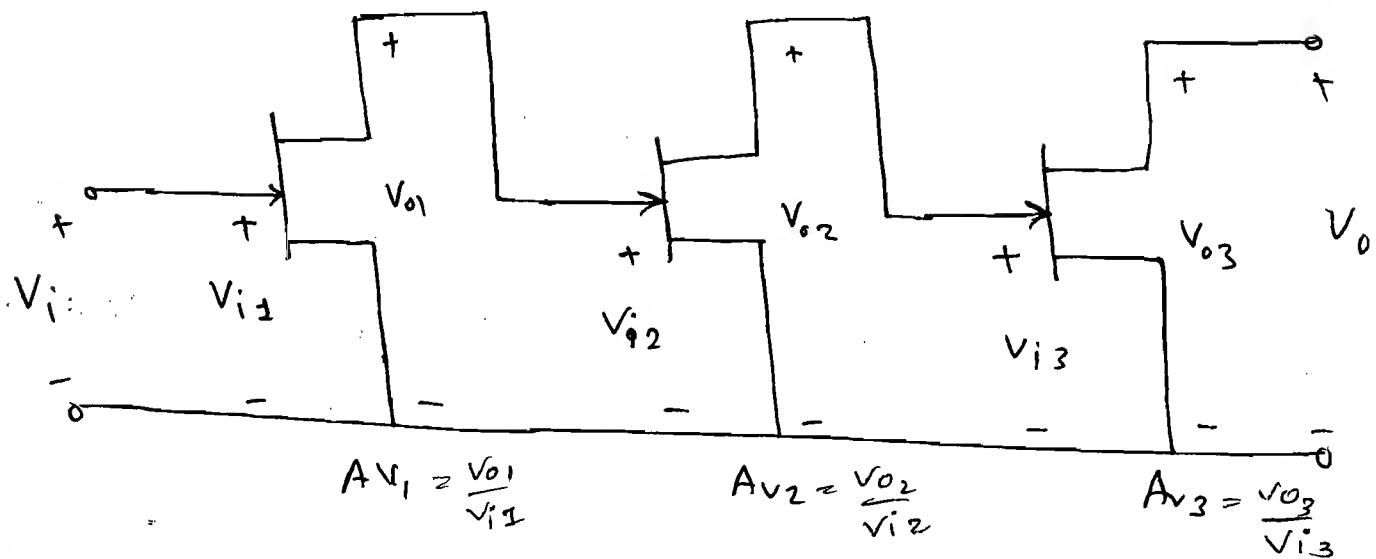
 $\Rightarrow \star$

\Rightarrow So, whenever we go for the multistage amplifier we should always remember it voltage gain and current.

Because voltage gain ~~excess~~ decide its input and output impedance. whenever we want to decide voltage amplifier max power should be transfer from one stage to another stage and for that MPTT should be used.

★ Multistage Amplifier:

⇒



Overall gain $A_v = \frac{V_o}{V_i}$

$$A_v = \frac{V_o}{V_i} = \frac{V_{o3}}{V_{i3}} \times \frac{V_{i2}}{V_{o2}} \times \frac{V_{i1}}{V_{o1}}$$

$$A_v = Av_3 \times Av_2 \times Av_1$$

⇒ In a multistage amplifier overall voltage gain is the product of individual stage voltage gain provided that there should not be any series resistance bet'n two stages but shunt resistance can be allowed.

⇒ In multistage current amplifiers overall current gain is the product of individual stage current gain provided that there should

33)

not be any shunt resistance b/w
 two stages but series resistor can be
 allowed.

\Rightarrow Multistage can be divided into four
 parts:

- ① Cascade
- ② Cascode
- ③ Darlington
- ④ Parallel.

① Cascade Connection: (for getting high voltage gain)

\Rightarrow For BJT:

CB: $\frac{Z_{in}}{\text{High}}$ $\frac{Z_o}{\text{Low}}$

CE: High High

CC: Low High.

we can connect

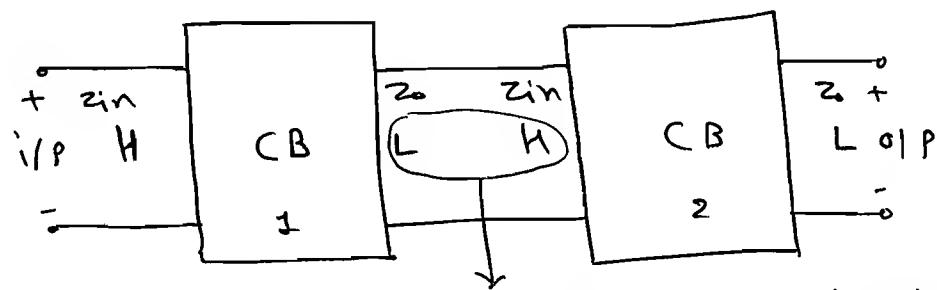
CB - CB

CE - CE

CC - CC.

} Possible but
 all are not
 valid.

① CB - CB:

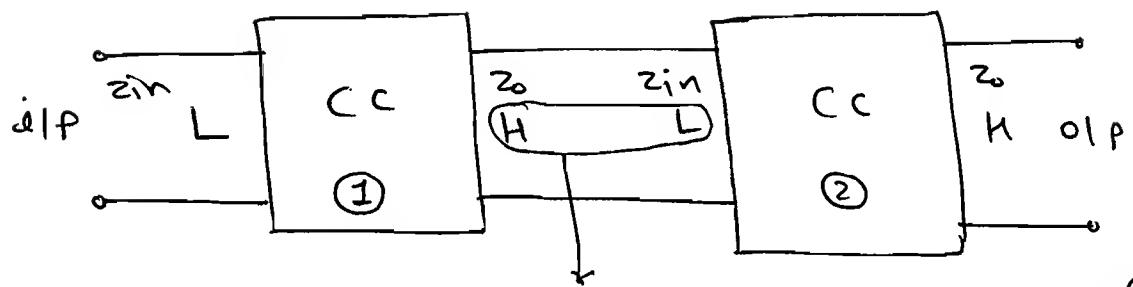


max. power not transfer from
 stage 1 to 2.

So, even though CB has high voltage gain
 it can not be used in cascade connection.
 for ^{overall} high voltage gain.

② CC - CC:

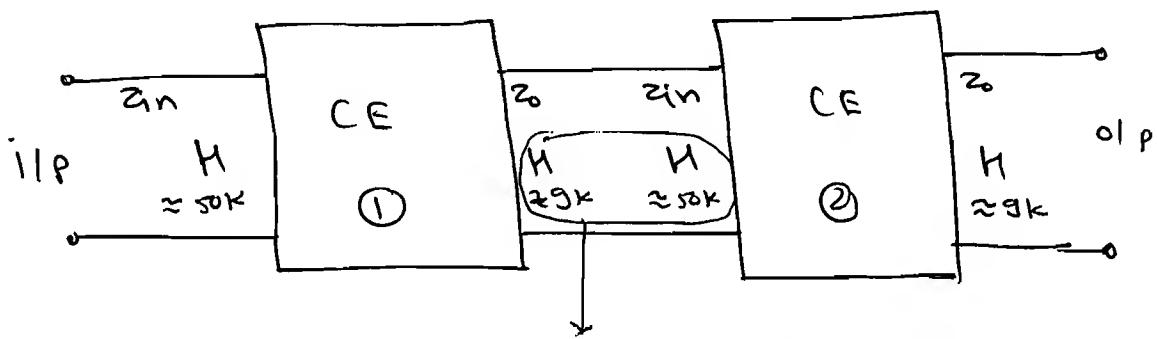
⇒



max. power will not be transferred
from stage ① to ②.

so, CC has voltage gain almost 1 and
and it also not used in voltage amp.

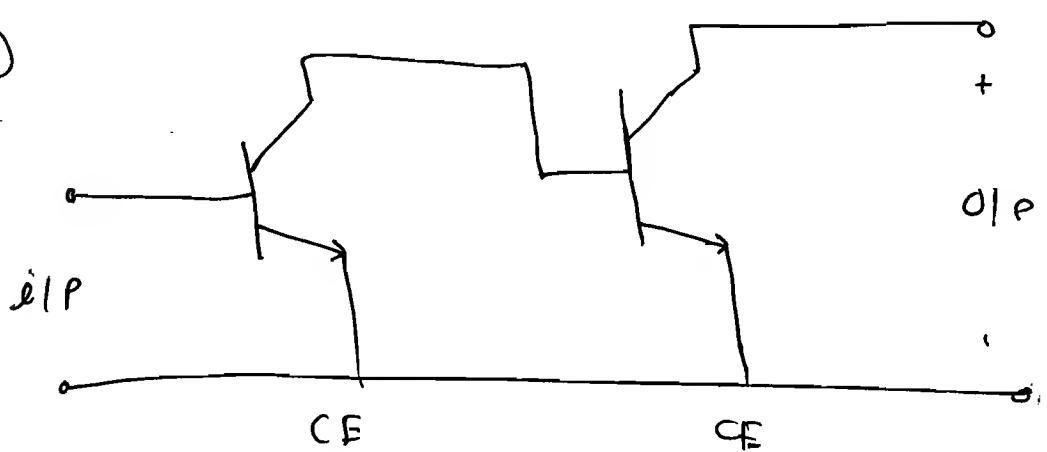
③ CE - CE:



due to this we can get max.
power transfer from stage -① to
②.

⇒ Therefore, In most of the practical
application we use CE - CE cascade amplifier.

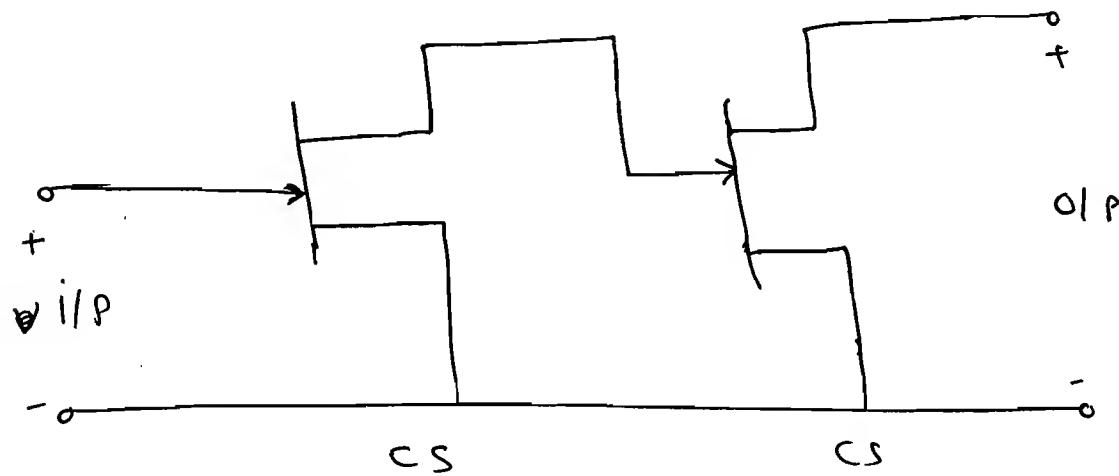
①



② For FET:

⇒ Same concept is applied into FET.

① So, only one possible way is CS-CS
Cascade connection for voltage amplifier.



② Cascade Connection: (for High Bandwidth & i/p impedance getting.)

⇒ ① For BJT:

CE CB CC

⇒ As there are three configuration (CE, CB, CC), there are six possible way to make cascade connection.

① CE - CB valid
H H L

~~CE~~

④ CB - CE
H H X H X not valid

② CE - CC invalid
H H X L H

⑤ CC - CE
L H L H valid

③ CB - CC valid
H L L H

⑥ CC - CB
L H H H valid

\Rightarrow Among six possibility, four are valid for wide band structure and case code connection.

From that,

we can say that $CB - CC$ & $CC - CB$ are same because it is a just matter of order. i.e. first CB (or) CC no matter, it work same.

\Rightarrow But, in $CB - CC$, input is $z_{in} = \text{high}$, $z_o = \text{high}$ whereas in

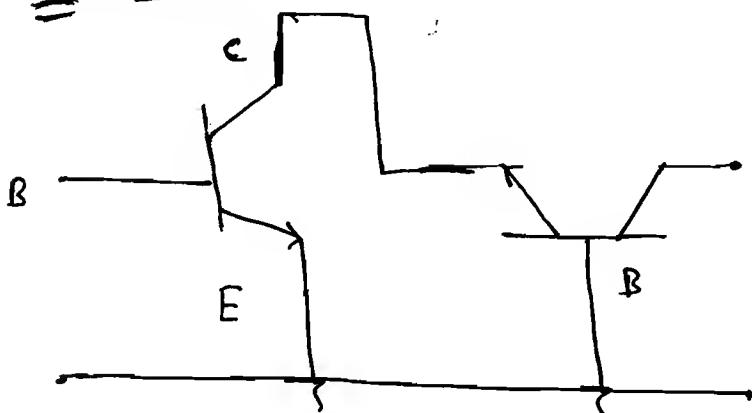
$CC - CB$

$z_{in} = \text{low}$, $z_o = \text{high}$. so it provides better gain compare to $CB - CC$.

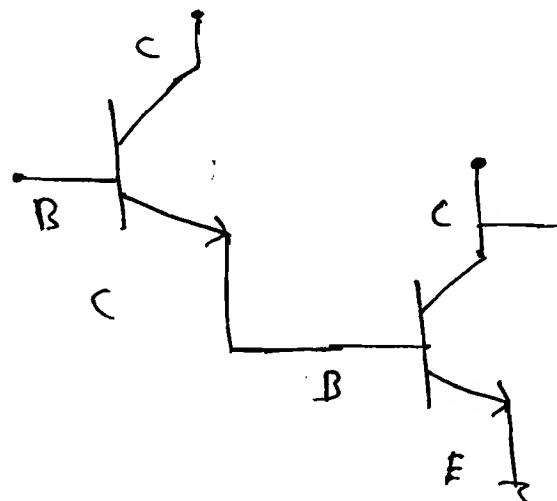
so, wide band structures (or) case code connections are.

- ① $CE - CB$
- ② $CC - CE$
- ③ $CC - CB$.

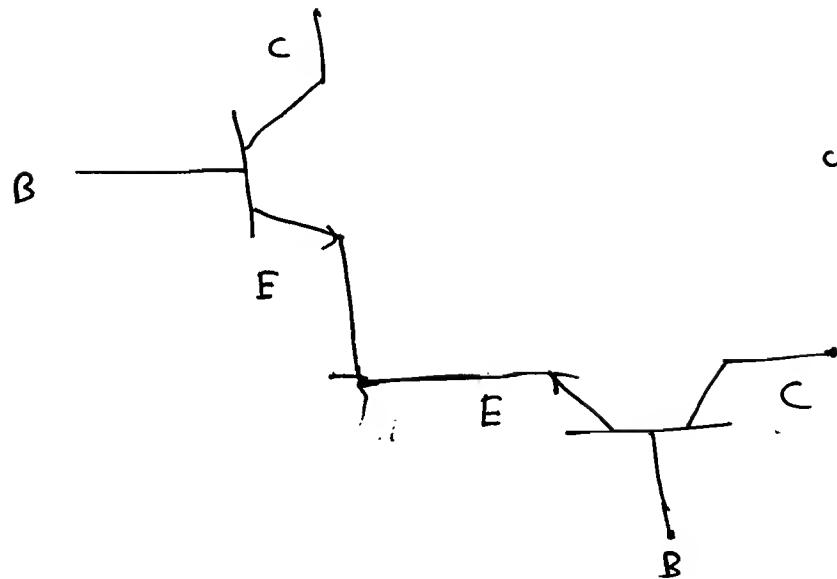
① $CE - CB$:



② $CC - CE$

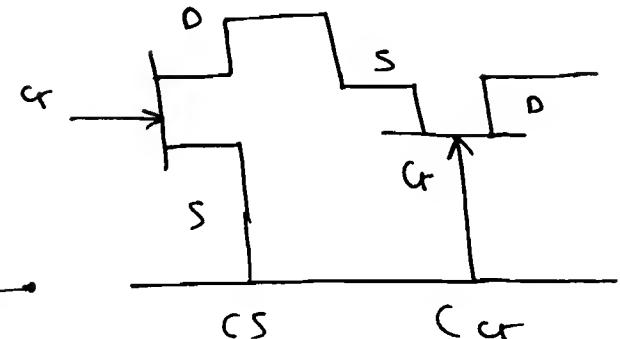


③ $C_{CE} - C_{CB}$:



② For JFET: 35)

\Rightarrow $C_S - C_{GS}$



$C_D - C_S$
 $C_D - C_{GS}$

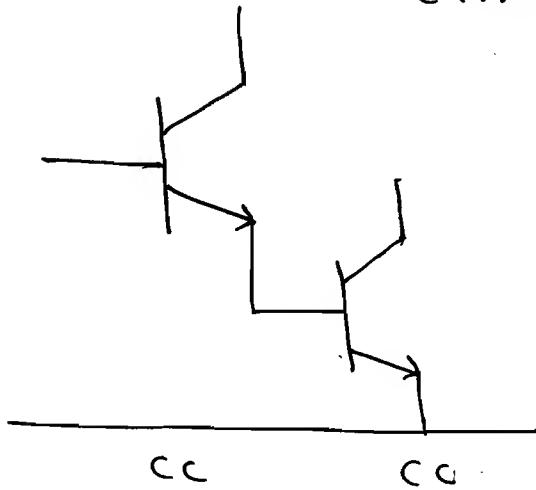
③

Demington Connection: (for getting high current gain)

① For BJT

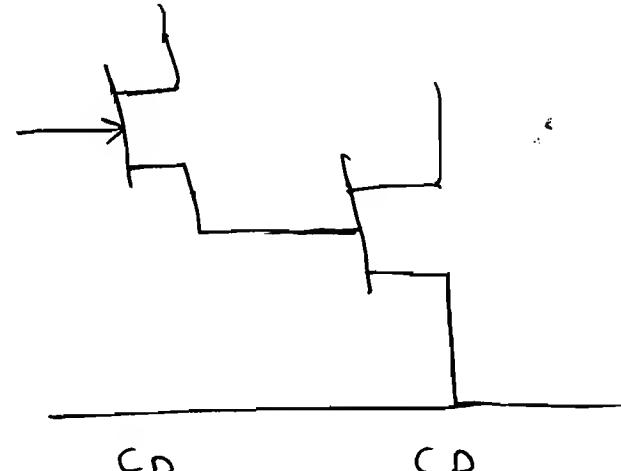
$C_{CE} - C_{CB}$

for large
current gain.



② for FET

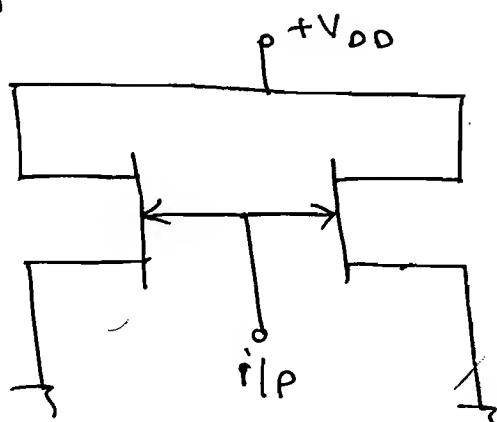
$C_D - C_S$



④

Parallel: (to increasing current Rating)

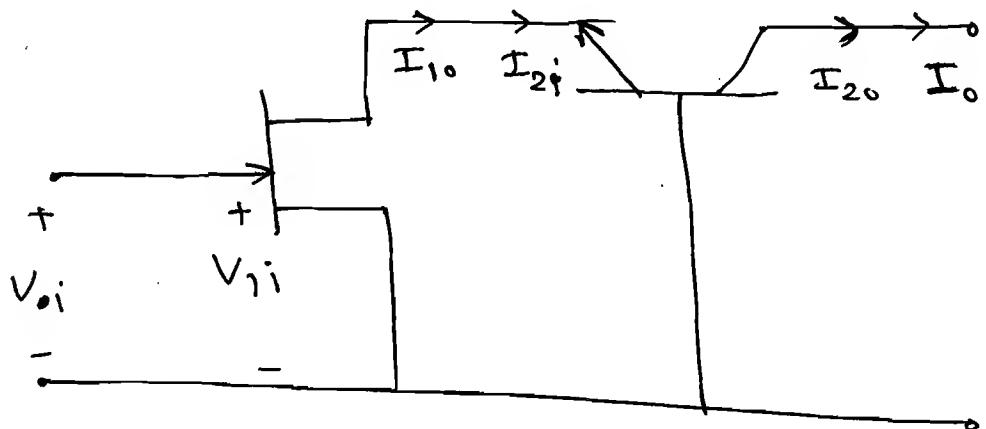
\Rightarrow FET



Q For the Ckt shown in the fig.

FET has transconductance of 5 mA/V and BJT has a ~~RB~~ CB current gain 0.8 .

Calculate overall transconductance of the composite amp.



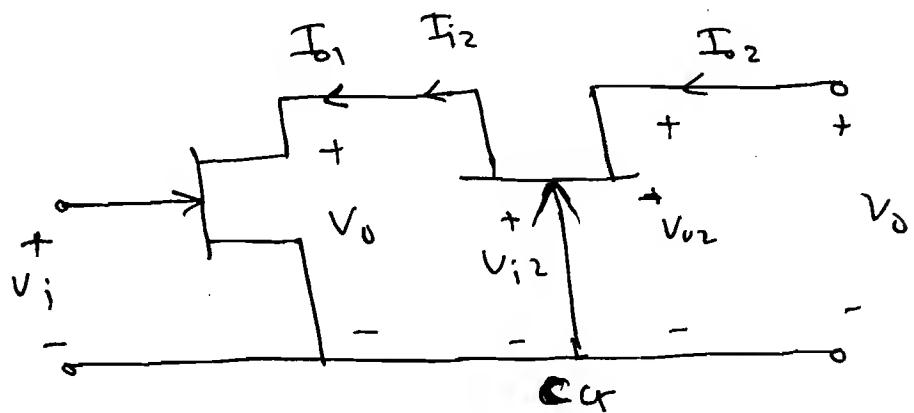
Sol:

$$\therefore g_m = \frac{I_o}{V_i} = \frac{I_o}{I_{2o}} \times \frac{I_{2o}}{I_{2i}} \times \frac{I_{2i}}{I_{1o}} \times \frac{I_{1o}}{V_{ii}} \times \frac{V_{ii}}{V_{oi}}$$

$$\therefore g_m = 0.8 \times 5$$

$$g_m = 4 \text{ mA/V.}$$

Q-2



\Rightarrow For the Ckt shown in the fig. transistor M₁ & M₂ has transconductances of g_{m1} & g_{m2} . Calculate the overall transconductance of the composite amplifier.

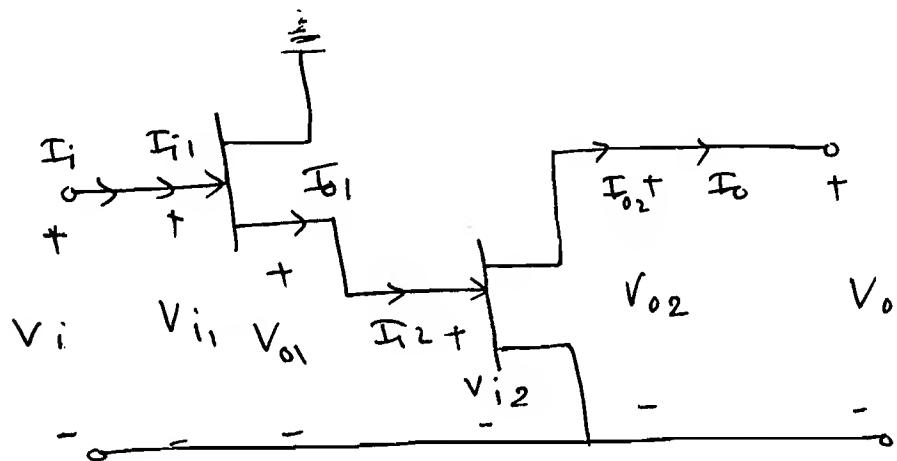
$$\Rightarrow \text{Overall } g_m = \frac{I_o}{I_{o2}} \times \frac{I_{o2}}{I_{i2}} \times \frac{I_{i2}}{I_o} \times \frac{I_{o1}}{V_{i1}} \times \frac{V_{i1}}{V_i} \quad 3c)$$

$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow$

$- \quad \ddot{\text{z}} \text{ (cur)} \quad 1 \quad g_m \quad 1$

$$g_m = g_{m1}$$

Q-3 For the Ckt. shown in the figure
 transistor M_1 & M_2 has transconductance
 of g_{m1} & g_{m2} . Calculate overall
 transconductance.



$$S_{01}^{in}: g_m = \frac{I_o}{V_i} = \frac{\frac{I_{o1}}{I_{o2}}}{\frac{V_{i2}}{V_{i1}}} \times \frac{\frac{V_{i2}}{V_{o1}}}{\frac{V_{o1}}{V_{i1}}} = g_{m1} \times g_{m2} \times \dots$$

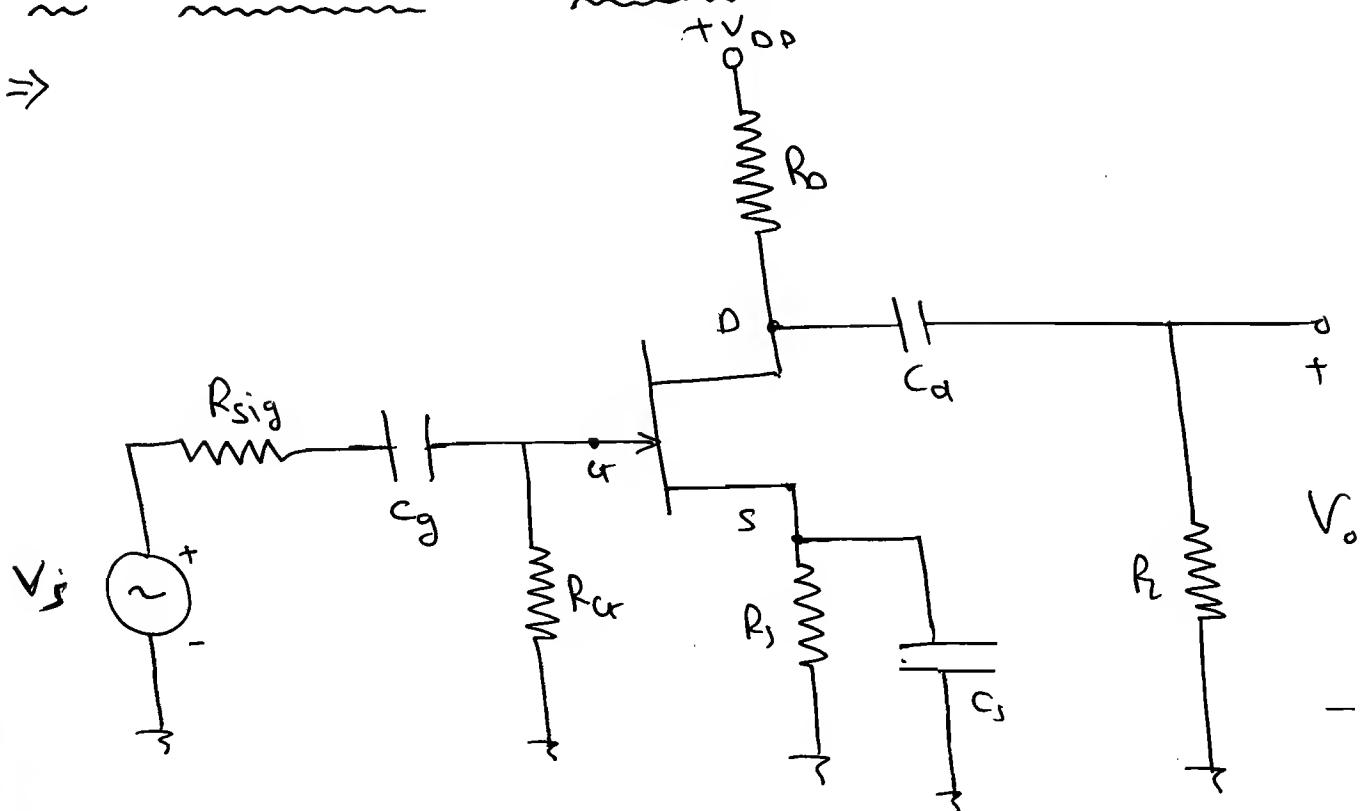


Frequency

⇒

Response

Analysis:



⇒ C_g, C_d & C_s : Coupling and bypass cap.

$$X_c = \frac{1}{\omega C} = \frac{1}{2\pi f C}$$

DC: $f = 0 \Rightarrow X_c = \infty$ so, o.c. for D.C.

* C_g :

⇒ It blocks the d.c. signals entering from source to input stage of the amplifier.

⇒ It blocks the d.c. signals entering from the 'i/p' stage of the amplifier to the source.

⇒ It isolates the input stage of the amp from the source d.c. point of view i.e. act like a open ckt for d.c. signals.

⇒ It couples the signals from source to

input of the amplifiers. i.e. it acts ³¹⁾ like a short circuit for a.c. signals.
⇒ It avoids the loading effect due to signal resistor

* C_d (MF)

⇒ It blocks the d.c. signals from the o/p stage of amplifier to the load.

⇒ It isolates the o/p stage of amp. from the load d.c. point of view. i.e. it acts like a open circuit ~~too~~ for the d.c.

⇒ It couples the a.c. signals from the o/p stage of amplifier to the load for a.c. signals.

* C_s :

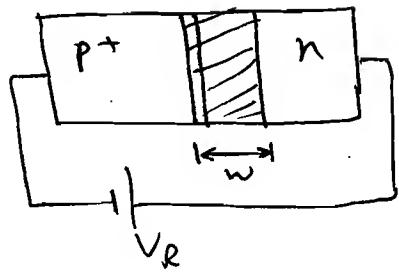
⇒ It avoids the -ve feedback due to source resistor R_s .

⇒ It bypasses a.c. signals through it.

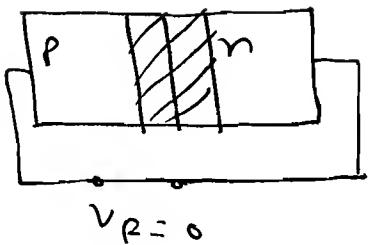
e.g. $C_d, C_s : (MF) (4.7 \mu F, 10 \mu F)$

→ Always prefer short circuit for a.c. signals.

① R.B.



② O.C.



$$\epsilon_0 = \epsilon A / w.$$

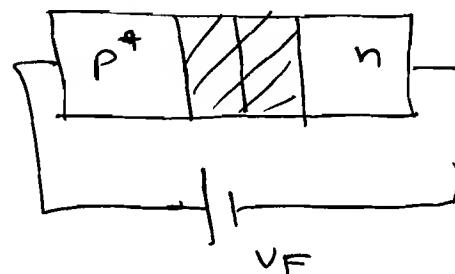
$$C = \frac{\epsilon A}{w}.$$

Transition Capacitance

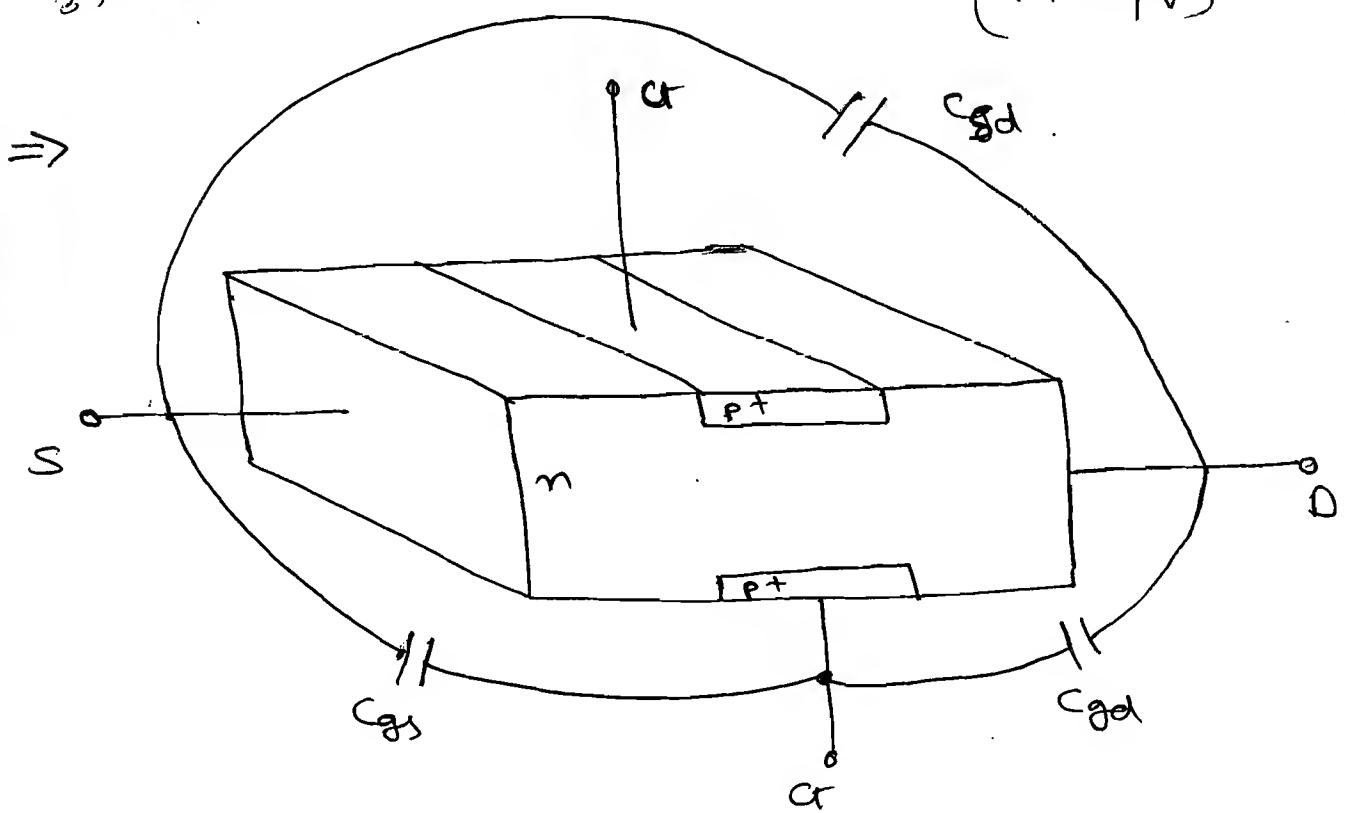
$$C_T = \frac{C_{T0}}{\left(1 + \frac{V_R}{V_0}\right)^{1/2}}$$

$1/2$ for linear

③ F.B. (Discussion Cap.).



$$C_j = \frac{C_{j0}}{\left(1 + V_R / V\right)^{1/2}}.$$



$\therefore C_{gs}, C_{gd} \& C_{ss}$: Junction Capacitors

\Rightarrow Always prefer open circuit for

$X_C = \frac{1}{\omega_C} = \frac{1}{2\pi f_C}$ cell A.C. signals.

$C_{gs}, C_{gd} (10^{-10} \text{ PF})$
 $C_{sd} (10^{-11} \text{ PF})$

* Low Freq.

⇒ Coupling Capacitor & Bypass Capacitor : O.C.
 ⇒ Junction Capacitors : O.C.

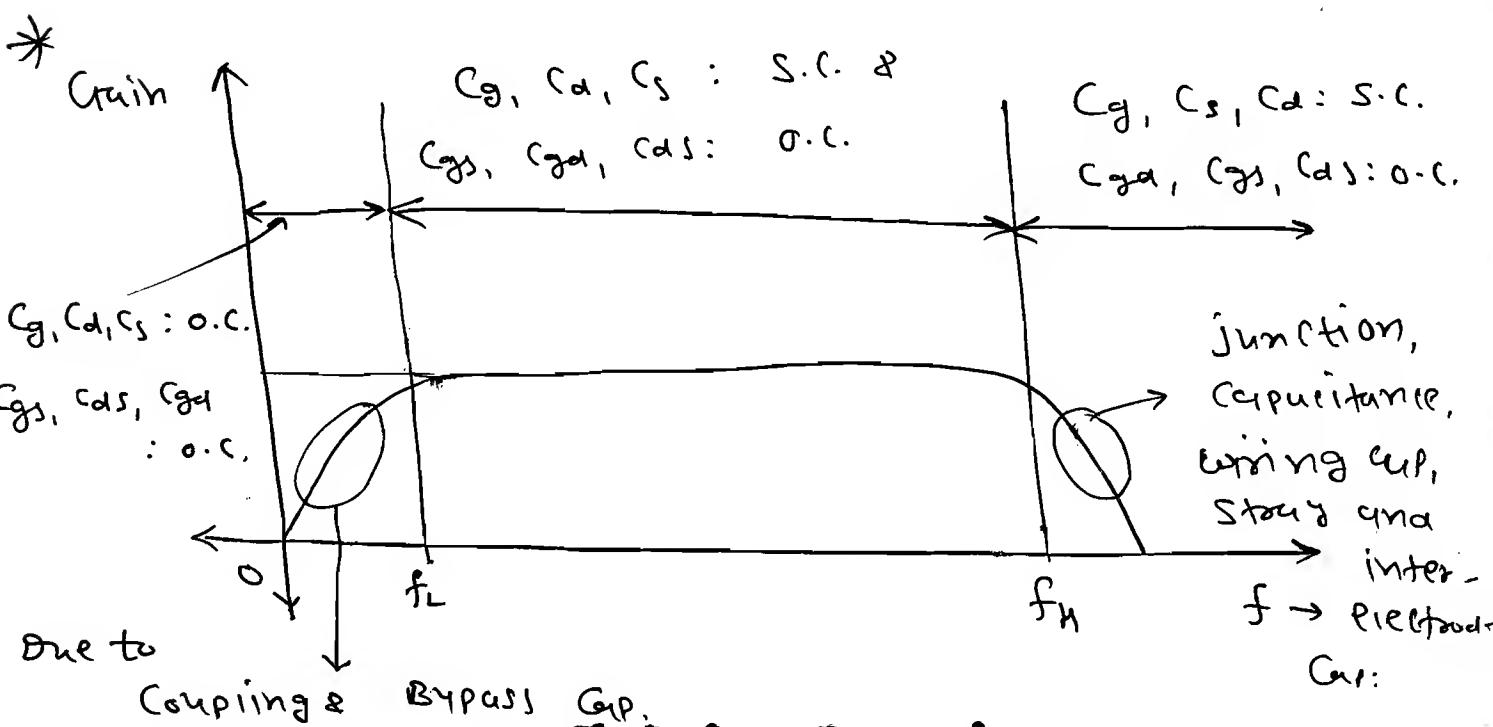
* Medium Freq.

⇒ Coupling Capacitor & Bypass Capacitor : S.C.
 ⇒ Junction Capacitors : O.C.

* High Freq.

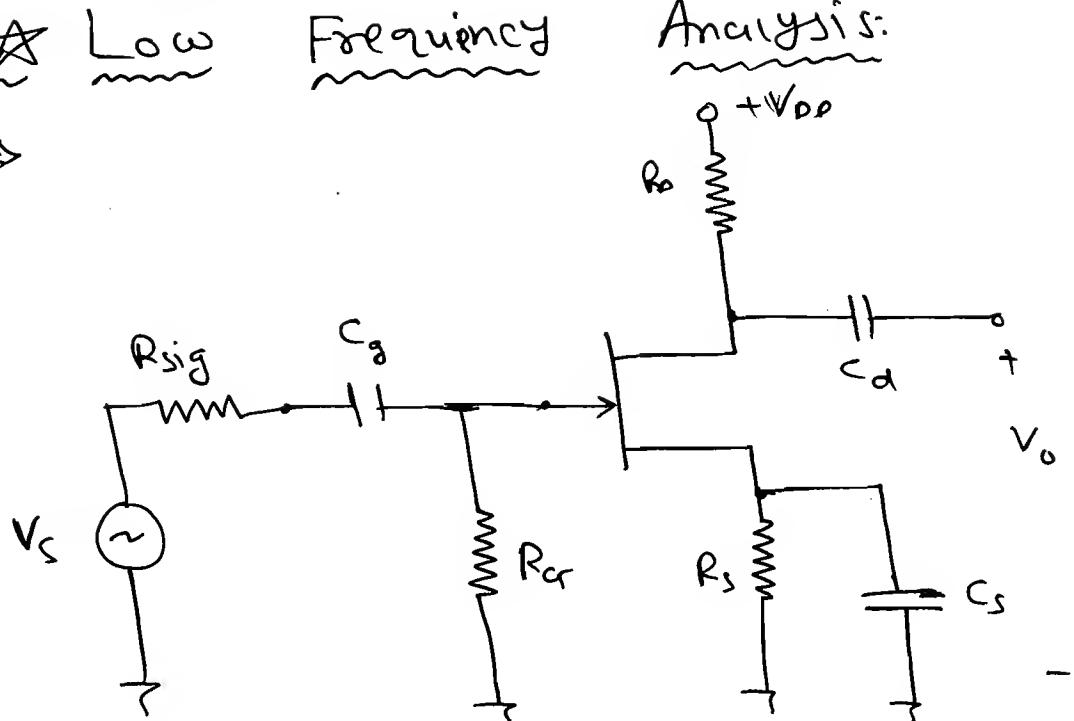
⇒ Coupling & Bypass Capacitors : S.C.
 ⇒ Coupling & Junction Capacitors : S.C.

Coupling & Bypass Capacitor		Junction Capacitors.
LF	O.C.	O.C.
MF	S.C.	O.C.
HF	S.C.	S.C.

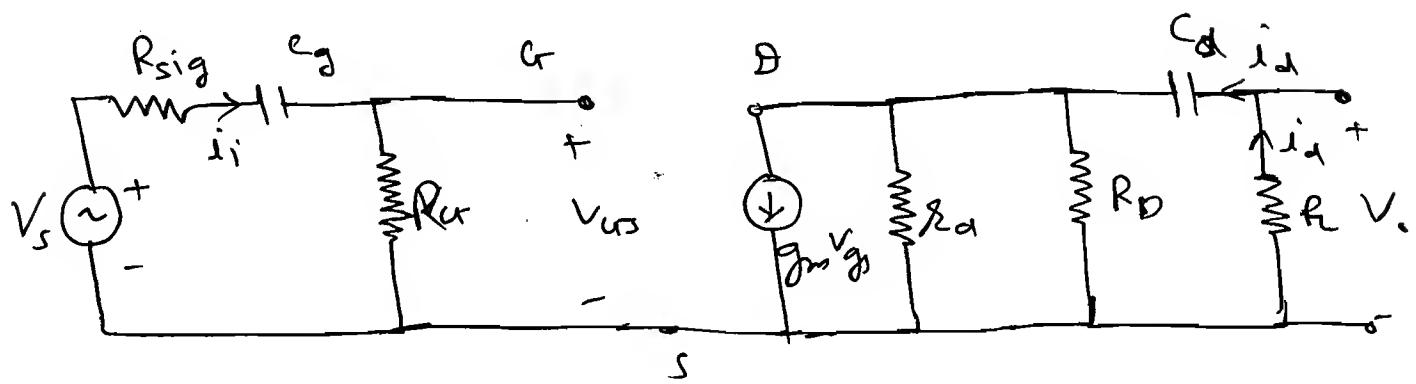


★ Low Frequency

⇒



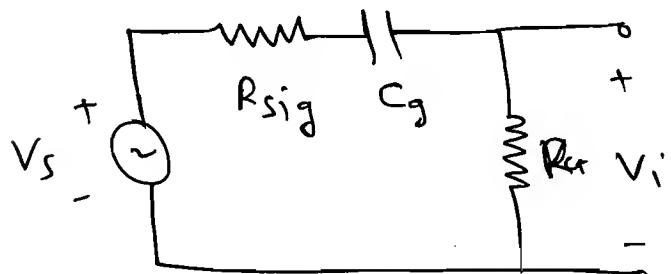
⇒ Small signal circuit



① Input side,

$$V_s = V_{sig} + V_{cg} + V_i$$

$$\Rightarrow V_i = V_s - V_{sig} - V_{cg}$$



$$H(j\omega) = \frac{V_i}{V_s} = \frac{R_{cr}}{R_{cr} + R_{sig} + j\omega C_g}$$

$$\therefore H(j\omega) = \frac{\frac{R_{cr}}{R_{cr} + R_{sig}}}{1 + \frac{1}{j\omega C_g (R_{cr} + R_{sig})}}$$

$$\Rightarrow H(j\omega) = \frac{A_0}{1 + j \frac{1}{2\pi f C_g (R_L + R_s j\omega)}}.$$

$$\therefore H(j\omega) = \frac{A_0}{1 + j \frac{f_L}{f}}.$$

where,

$$f_L = \frac{1}{2\pi C_g (R_L + R_s j\omega)}$$

$$|H(j\omega)| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}.$$

as $C_d < C_g < C_s$.

$$\Rightarrow f_d > f_g > f_s.$$

✓

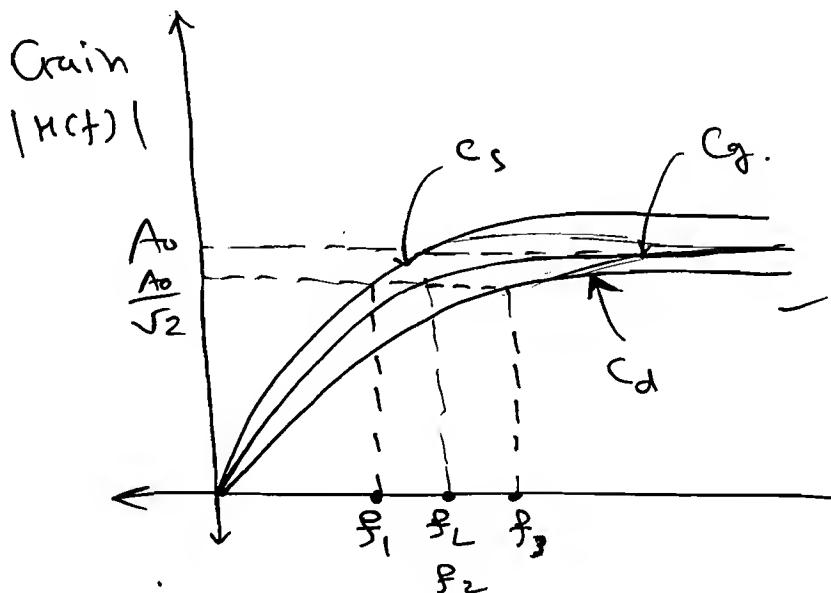
so $f_L = f_d$,
 $= f_{L3}$.

$$\Rightarrow f=0 \Rightarrow H(j\omega)=0.$$

$$f = f_s \Rightarrow H(j\omega) = A_0 / \sqrt{2}.$$

$$f = f_d = \omega \Rightarrow |H(j\omega)| = A_0.$$

\Rightarrow

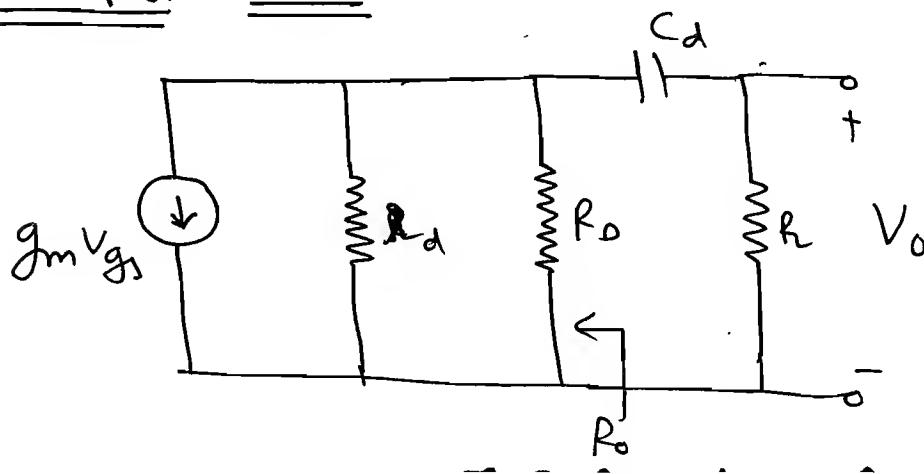


$$f_L = f_{L3}.$$

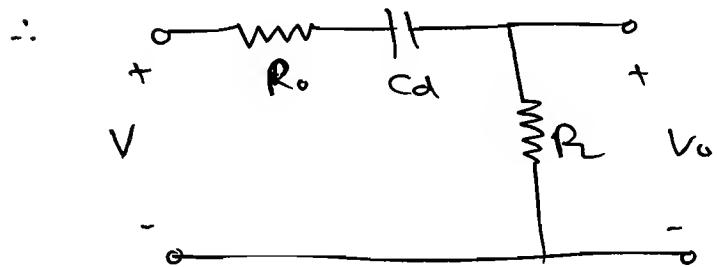
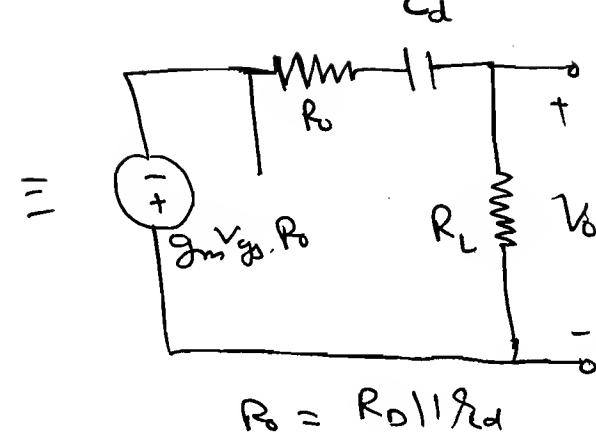
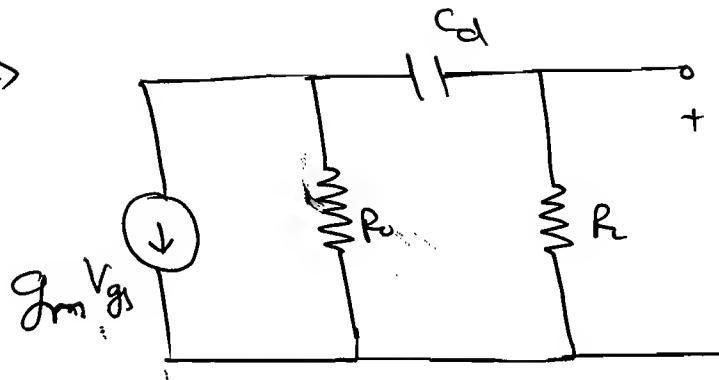
(lower cut-off freq.)

i.e. due to
 C_d .

② Output side:



\Rightarrow



$$\Rightarrow H(f) = \frac{R_L}{R_0 + R_L + \frac{1}{j f 2\pi C_d}}.$$

$$H(f) = \frac{\frac{R_L}{R_0 + R_L}}{1 + \frac{1}{j f 2\pi C_d (R_0 + R_L)}}.$$

$$\therefore H(f) = \frac{A_L}{1 + j \left(\frac{f_L}{f} \right)^2}.$$

$$\therefore |H(f)| = \frac{A_L}{\sqrt{1 + \left(\frac{f_L}{f} \right)^2}},$$

$$f_L = \frac{1}{2\pi C_d (R_0 + R_L)}.$$

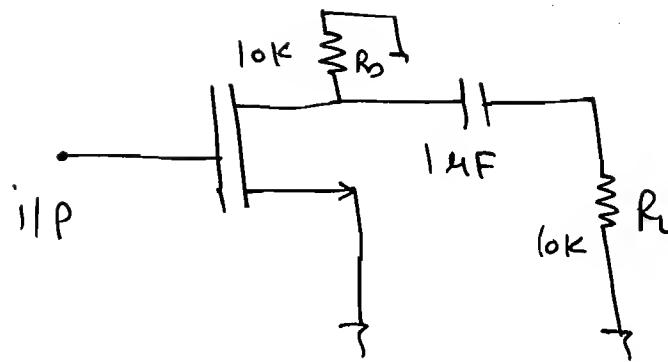
if C_s is present, then

~~work~~

$$\therefore f_L = \frac{1}{2\pi C_s R_{eq}}$$

$$R_{eq} = R_s \parallel \frac{1}{g_m}.$$

Q - 2M
2013 ECE



find f_L ?

40)

Sol'n:

$$f_L = \frac{1}{2\pi C_B (R_B + R_L)} = \frac{1}{2\pi \times 10^{-6} \times 20 \times 10^3}$$

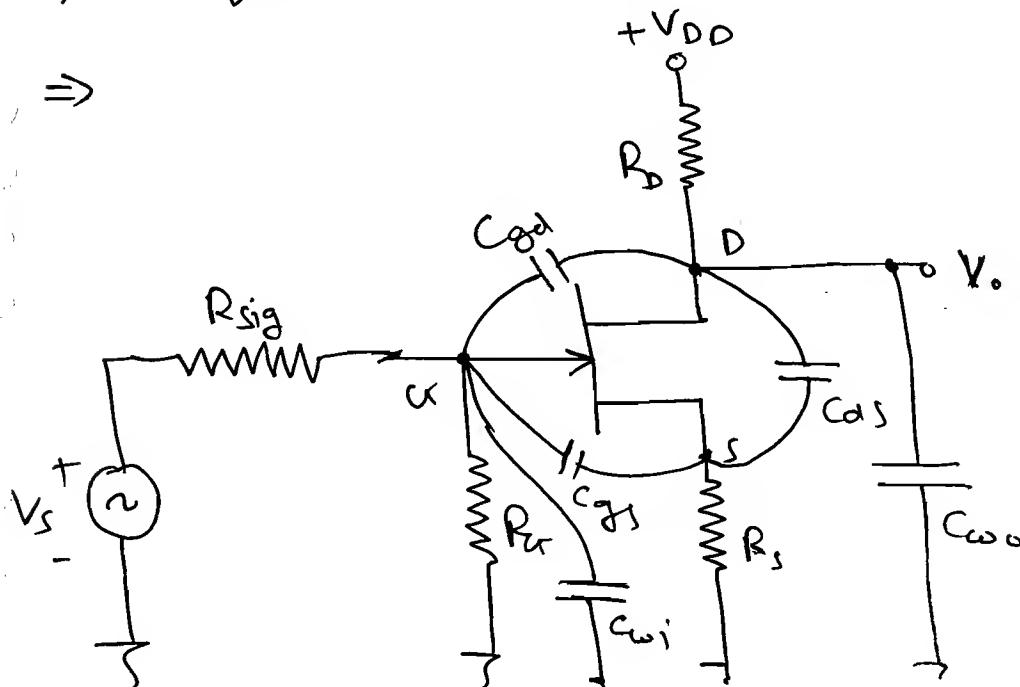
$$\therefore f_L = 7.96 \text{ Hz}$$

 High Frequency

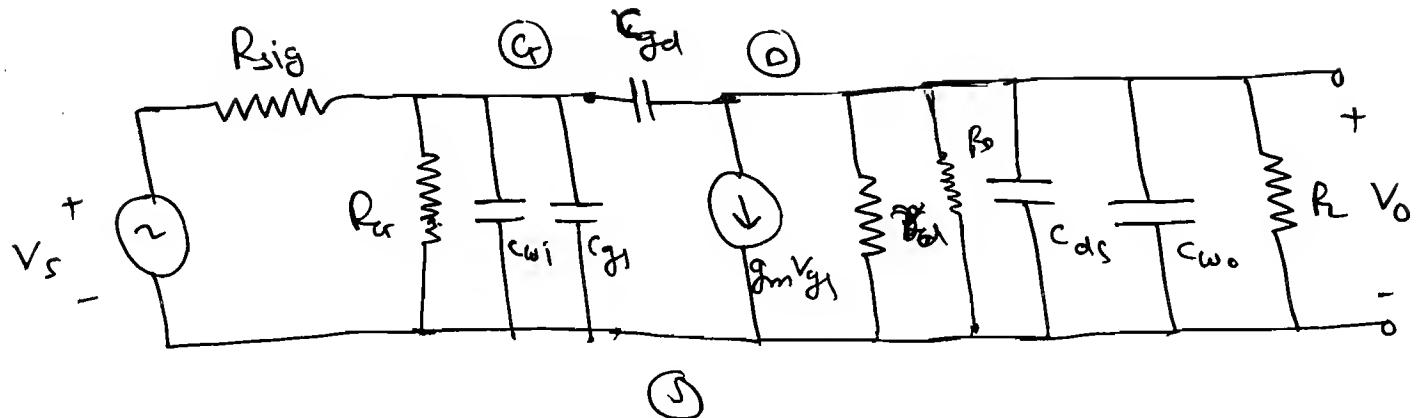
Analysis:

\Rightarrow At low freq. amplifier behaves like a high pass filter due to coupling and bypass capacitor. Therefore gain falls at low freqs. due to coupling and bypass cap.

\Rightarrow

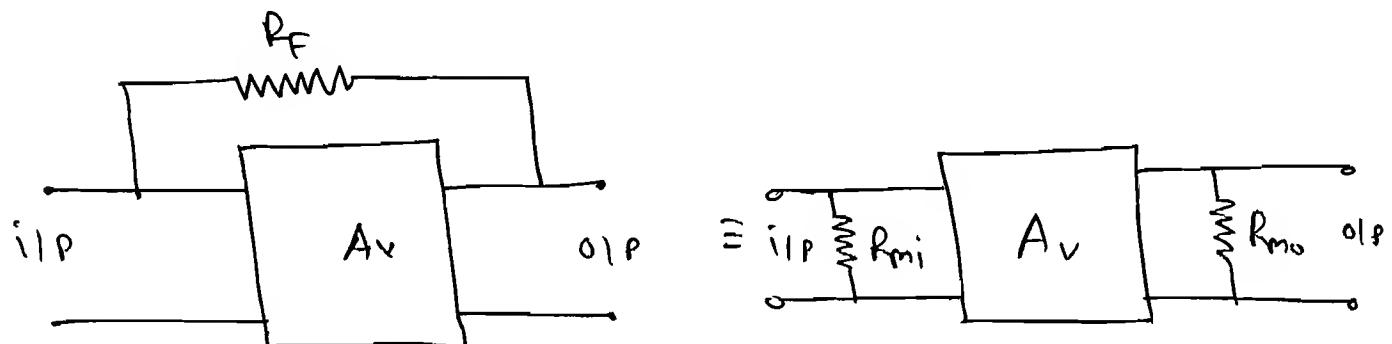


\Rightarrow Small Signal or CKT:



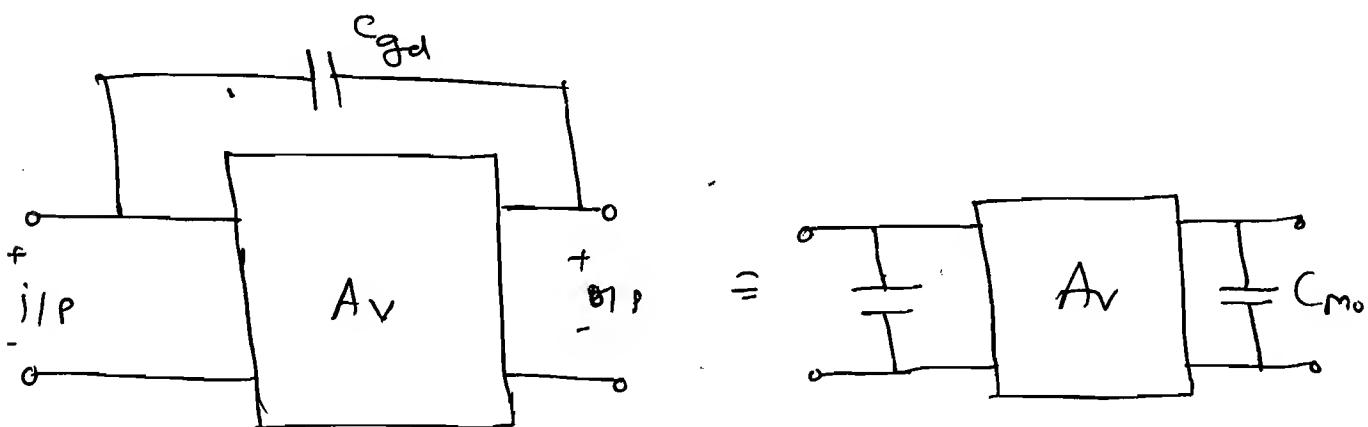
* Miller's theorem:

⇒



$$R_{ni} = \frac{R_F}{1 - A_V}, \quad R_{no} = \frac{R_F}{1 - \frac{1}{A_V}} \approx R_F \quad \text{for large voltage gain.}$$

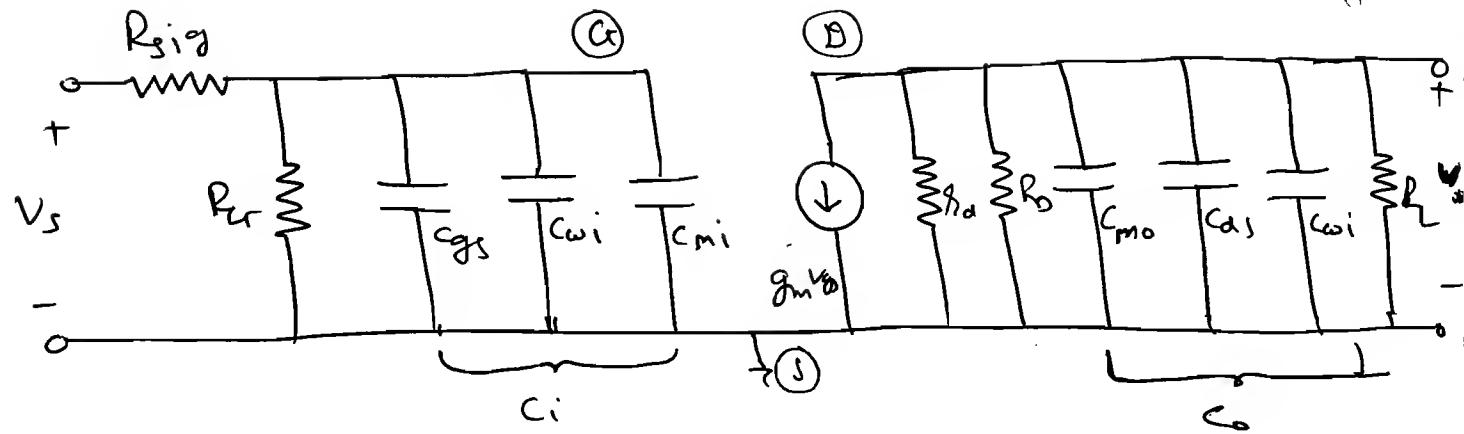
A thick black arrow pointing to the right, indicating a continuation or next step.



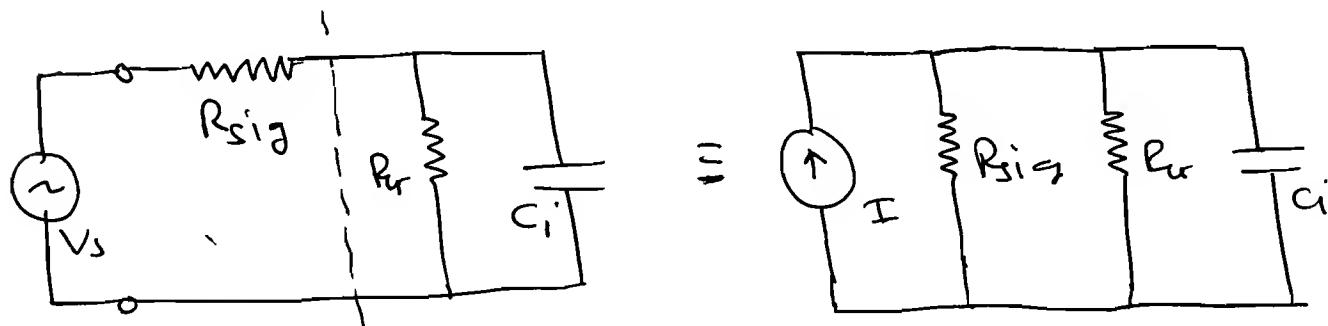
$$\Rightarrow C_{mi} = C_{gd} (1 - A_r).$$

$$C_{m0} = C_{ga} \left(1 - \frac{1}{Ar} \right) \approx C_{ga}.$$

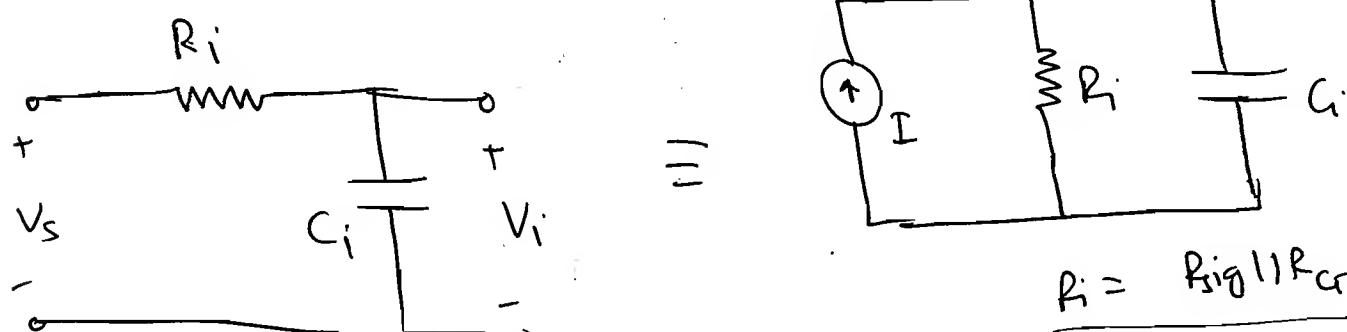
for large value of A



① Input side:



$$C_i = C_{gs} + C_{oi} + C_{mi}$$



$$\Rightarrow H(j\omega) = \frac{\frac{1}{j\omega C_i}}{R_i + \frac{1}{j\omega C_i}}$$

$$H(j\omega) = \frac{1}{1 + j\omega C_i R_i}$$

$$\therefore H(f) = \frac{1}{1 + j f 2\pi C_i R_i}$$

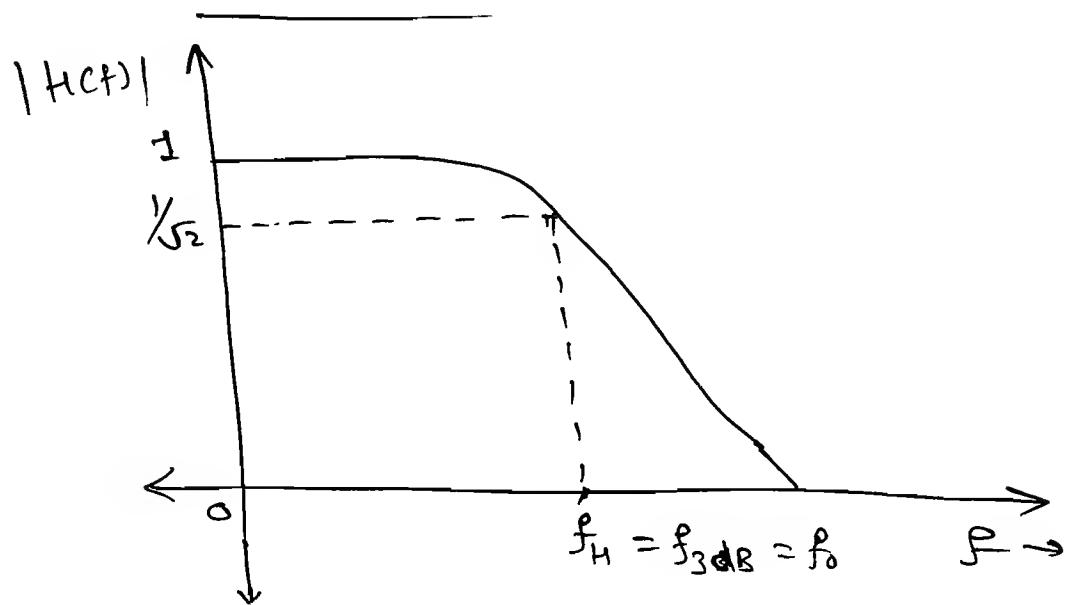
$$H(f) = \frac{1}{1 + j \frac{f}{f_H}} \Rightarrow |H(f)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}$$

$$\therefore f_H = \frac{1}{2\pi C_0 R_0}$$

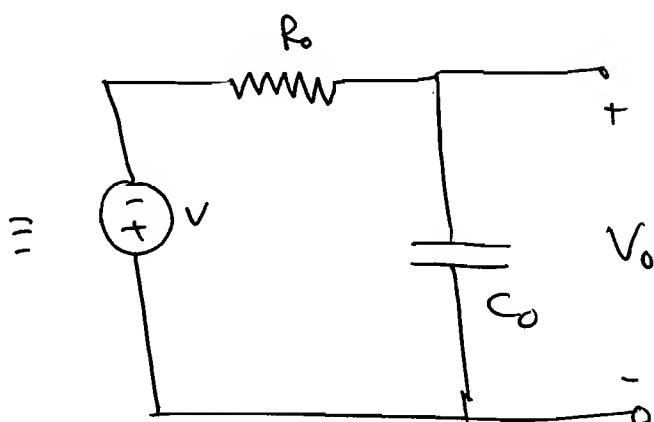
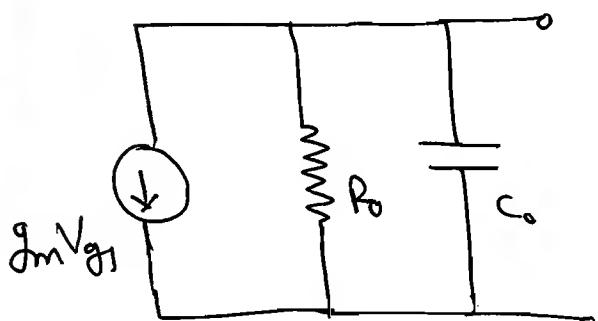
\Rightarrow for $f = 0 \Rightarrow |H(f)| = 1$.

for $f = f_H \Rightarrow |H(f)| = 1/\sqrt{2}$.

for $f = \infty \Rightarrow |H(f)| = 0$.



② O/P Side:



$$H(f) = \frac{1}{1 + j f 2\pi C_0 R_0}$$

$$h(f) = \frac{1}{1 + j \frac{f}{f_H}}$$

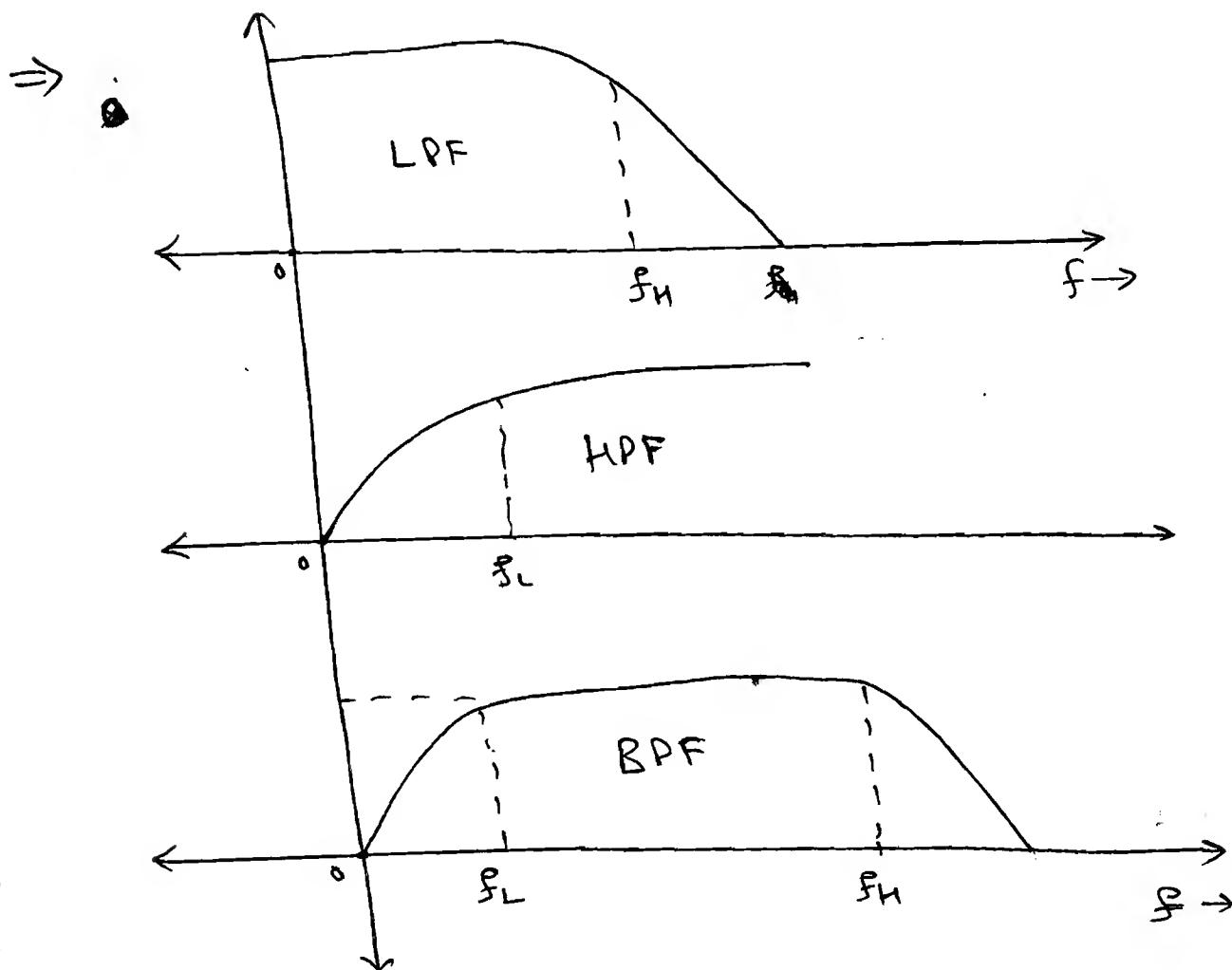
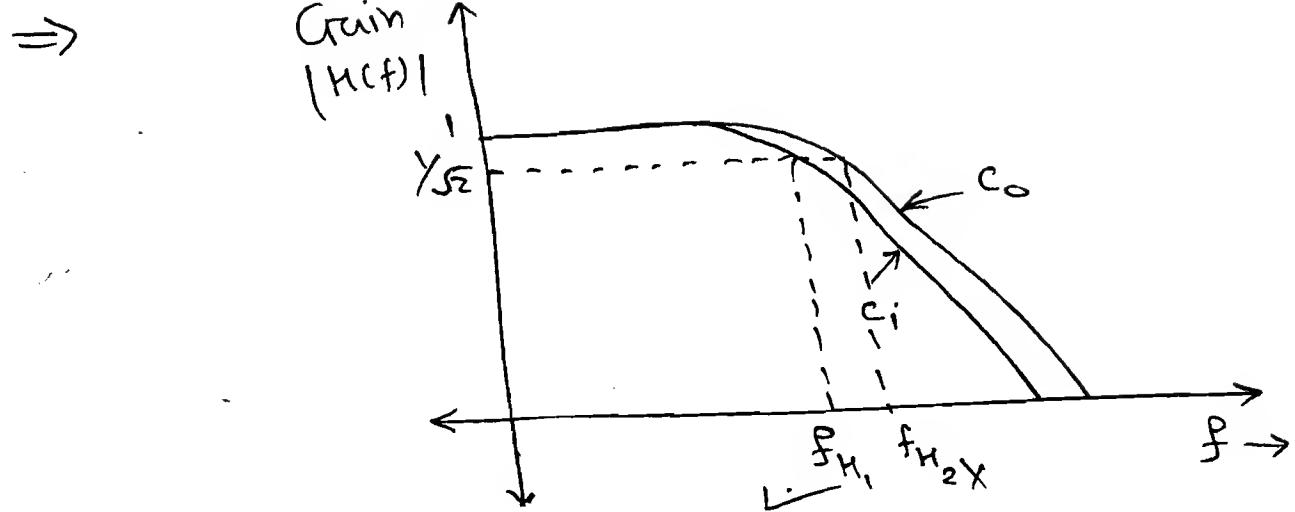
$$\therefore |H(f)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}}$$

$$R_0 = R_L \parallel R_d \parallel R_0$$

$$R_0 = R_L \parallel R_0 \quad (\because R_d \gg R_0)$$

$$C_0 = C_{m0} + C_{w0} + C_{ds}$$

$$f_H = \frac{1}{2\pi R_0 C_0}$$

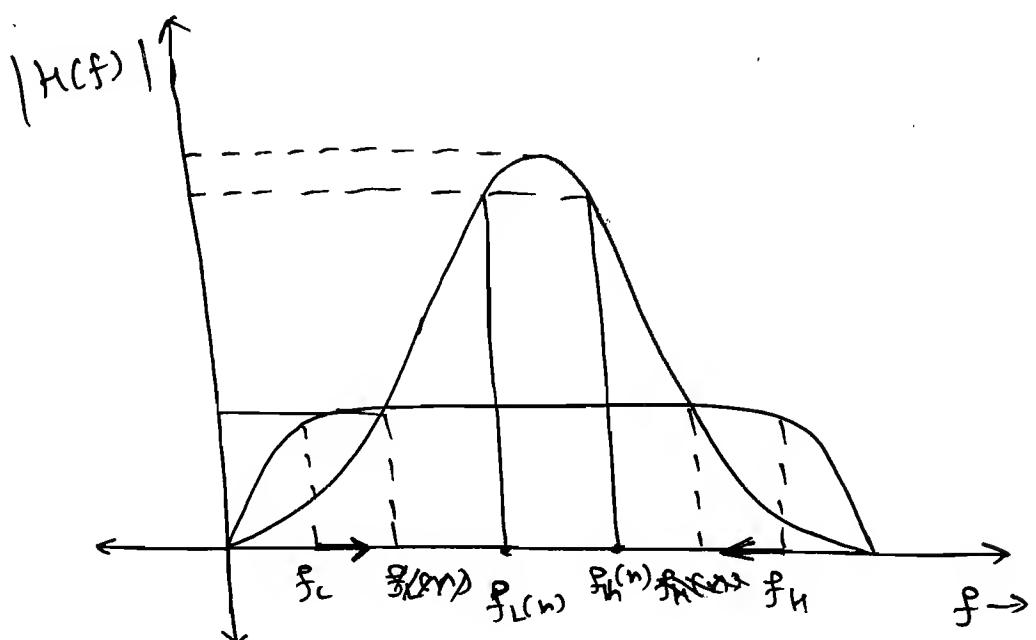


⇒ At high freq. Amp. behaves like a LPF due to junction, wiring, stray and inter-electrode capacitance. Therefore, gain falls at high frequency due to junction, wiring, stray and interelectrode capacitors.

\Rightarrow Amplifier is behaving like a hPF at Low freq. and is behaving like a LPF at high freq. Therefore, amplifier is

" BPF.

\Rightarrow



$$Bw = f_H - f_L$$

$$f_L(n) = \frac{f_L}{\sqrt{2^n - 1}}$$

$$f_H(n) = f_H \sqrt{2^n - 1}$$

$$Bw(n) = f_H(n) - f_L(n)$$

$$BW(n) = B.W. \sqrt{2^n - 1}$$

* Drawback of JFET:

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⇒ more gate leakage current.
i.e. more I_{GS}

⇒ large size.

⇒ V_{DS} & V_{GS} have different polarities.

n-JFET

V_{GS} : +ve

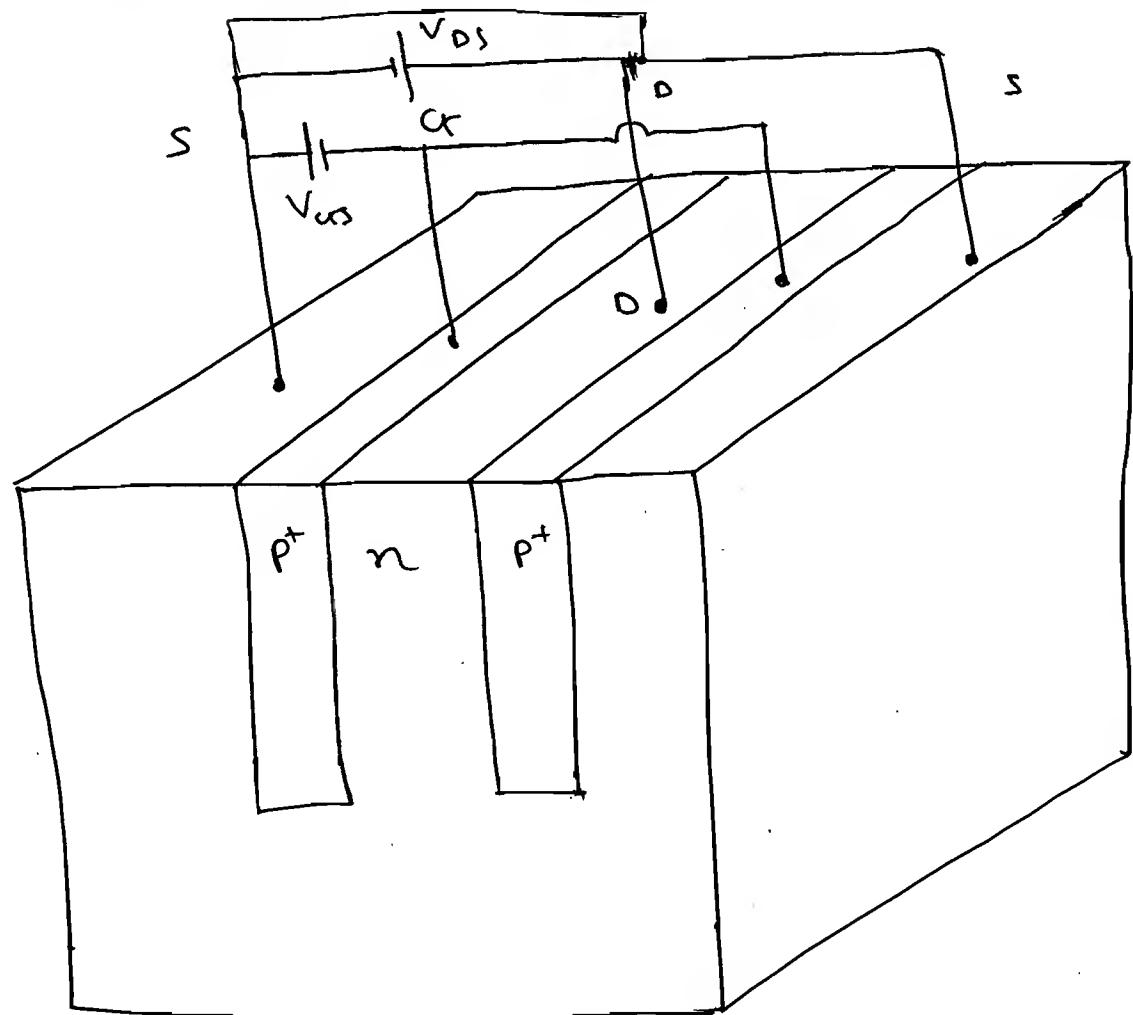
V_{DS} : -ve

P-JFET

V_{DS} = -ve

V_{GS} = +ve.

⇒ Now, a days following constⁿ of FET is used.



★ Depletion

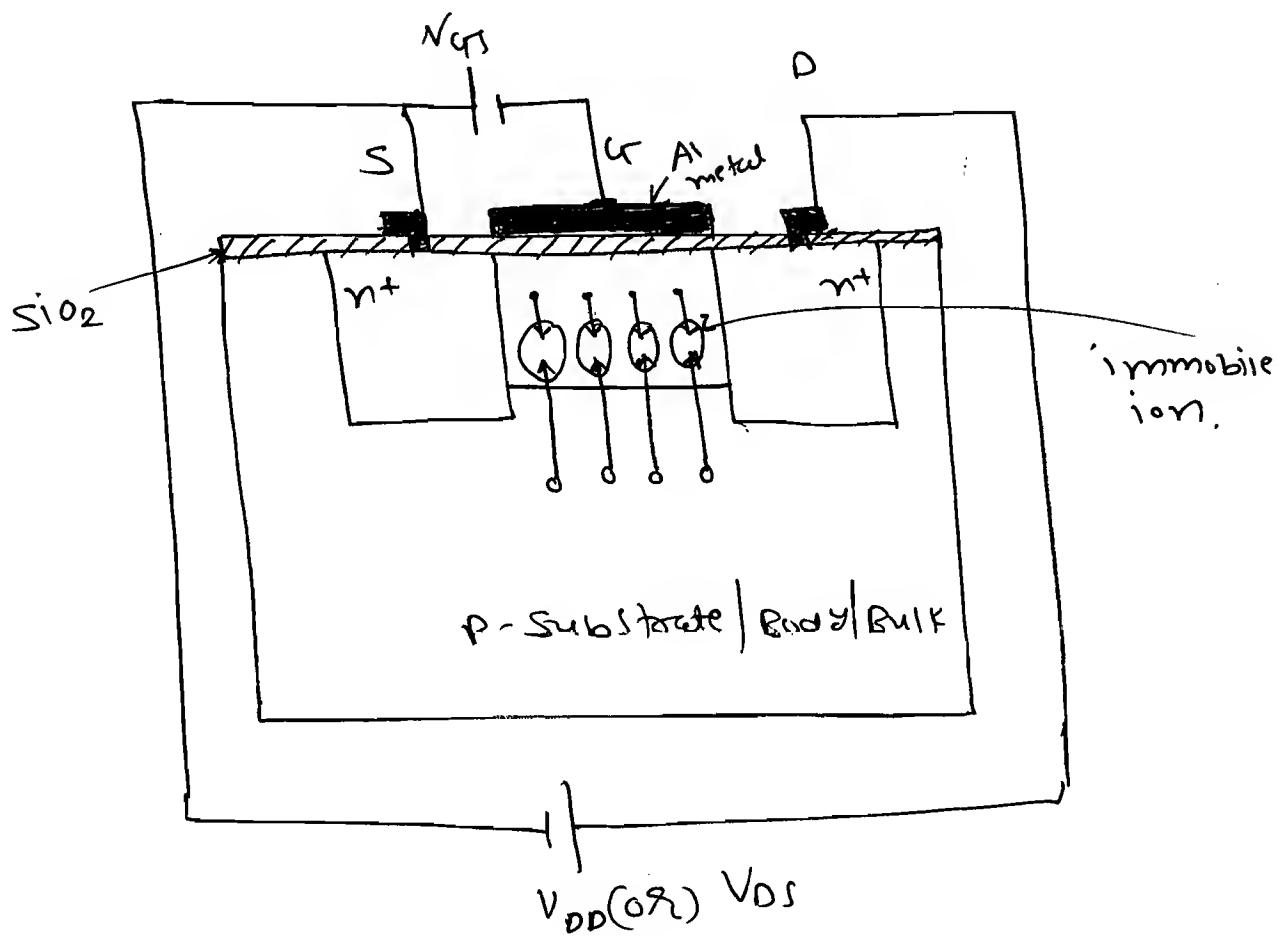
MosFET:

① n- channel

Depletion

MosFET: (n- DMosFET)

⇒

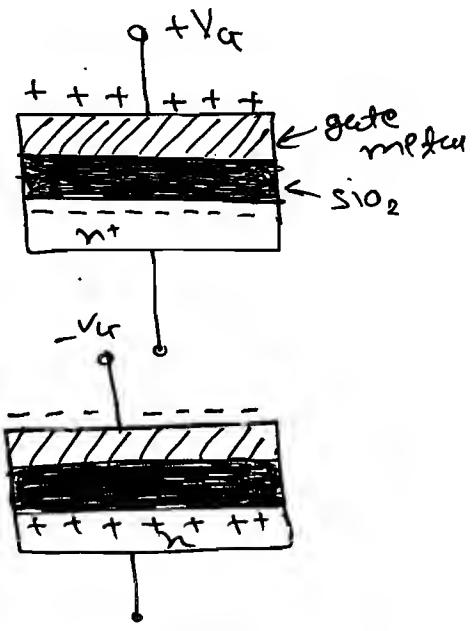
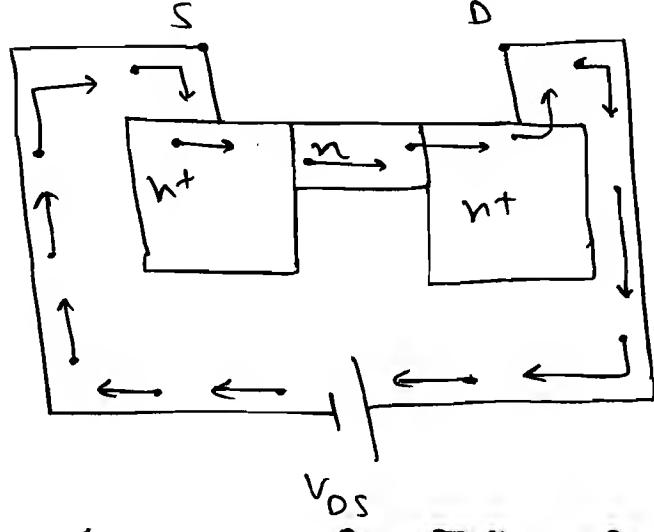


$$\Rightarrow R_{iBJT} < R_{iJFET}$$

$$R_{iJFET} < R_{imosFET}$$

$$\therefore R_{iBJT} < R_{iJFET} < R_{imosFET}.$$

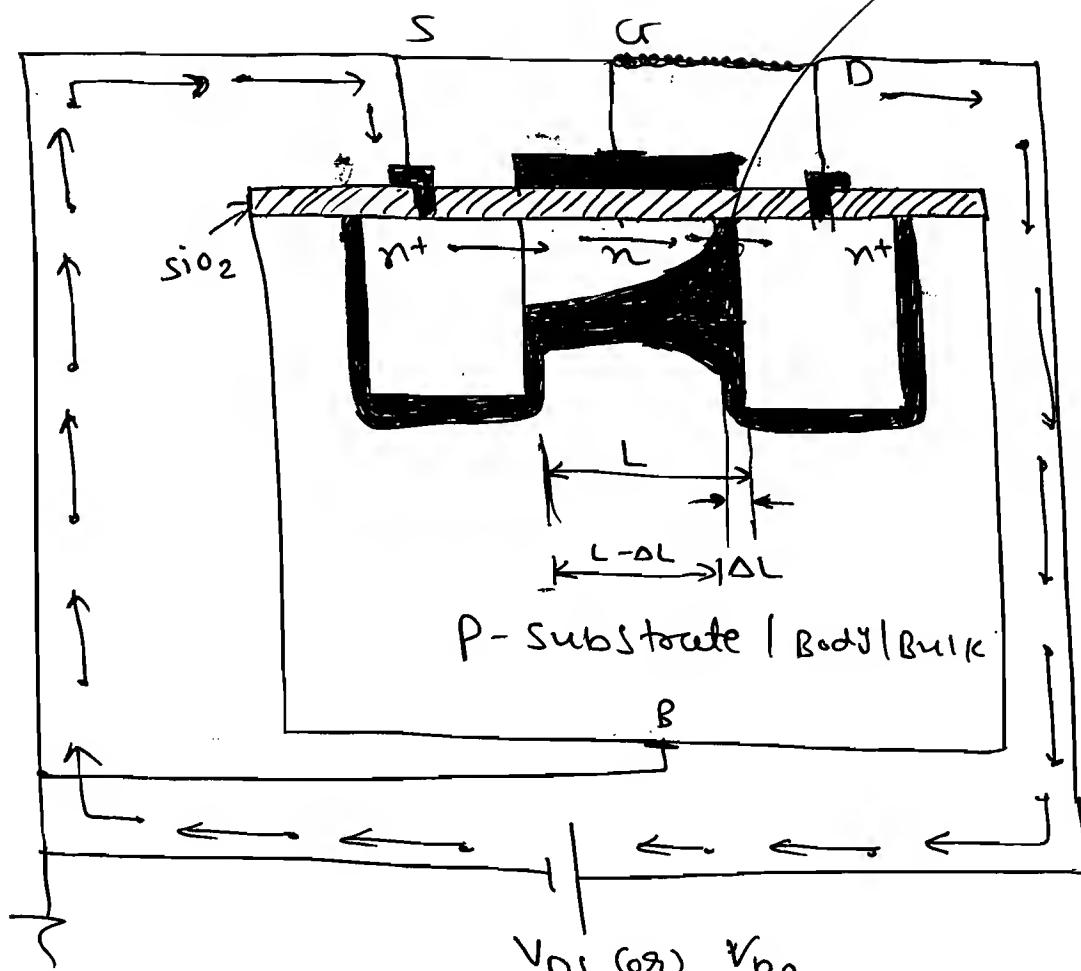
⇒



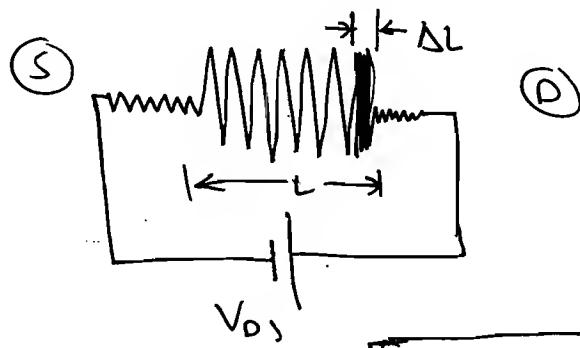
Case -i): $\text{Vars} = 0.$

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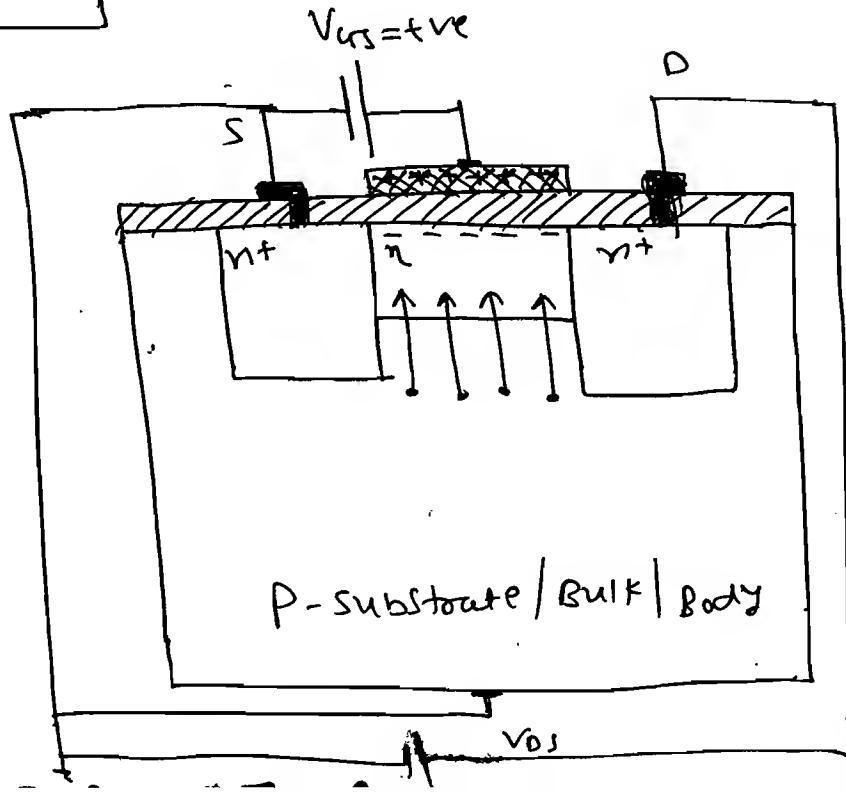
pinch-offs



$$E = \frac{V_{DS}}{L}$$

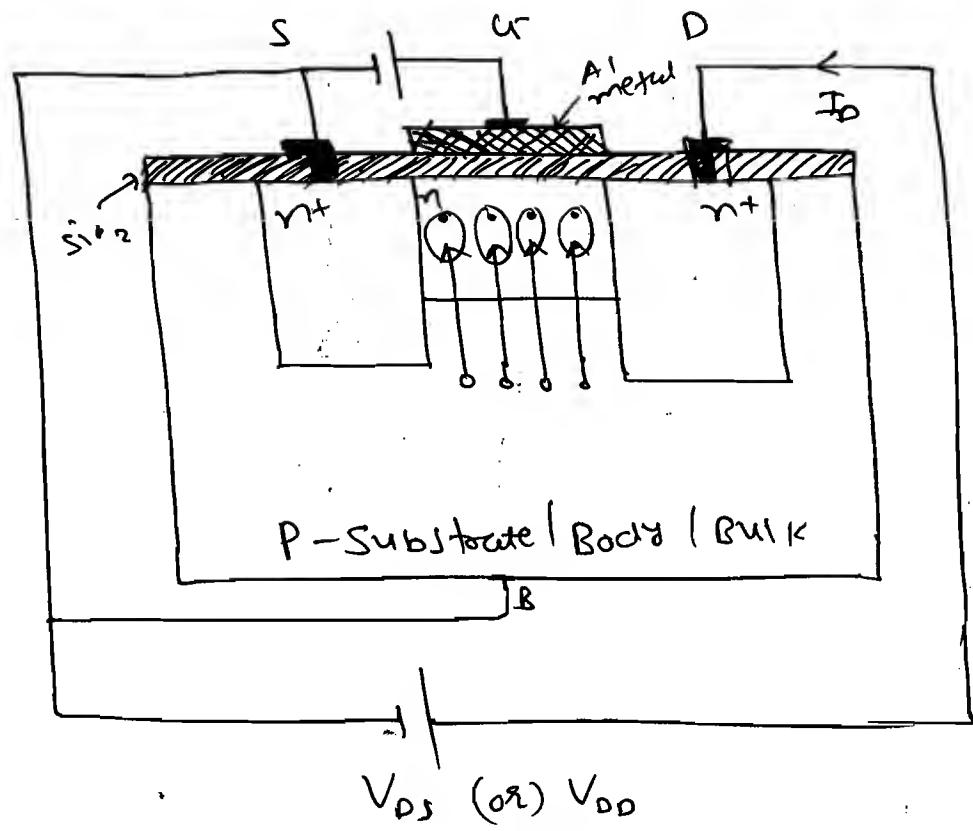


case - (i) $V_{CS} = +ve.$

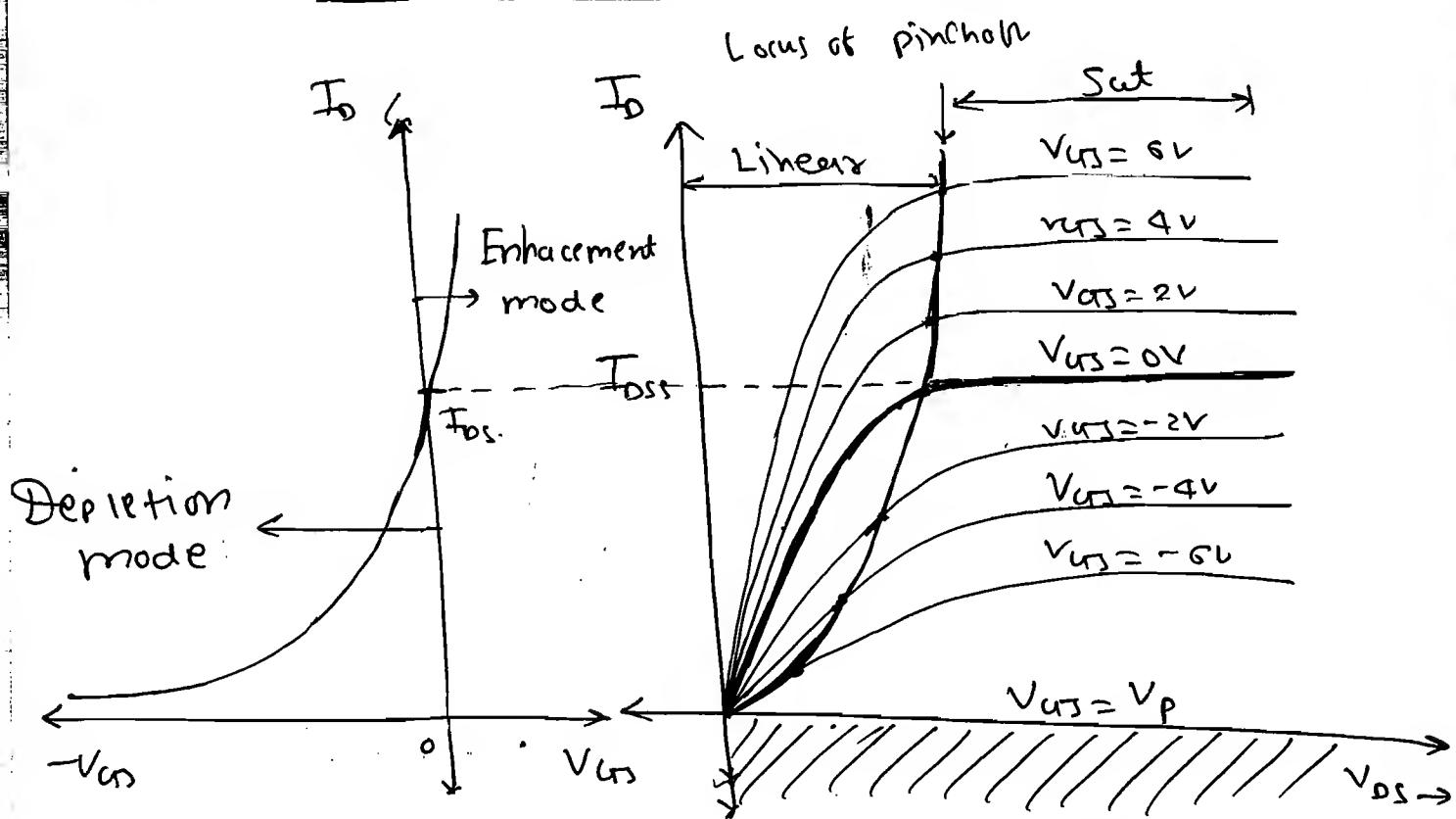


Case-(iii)

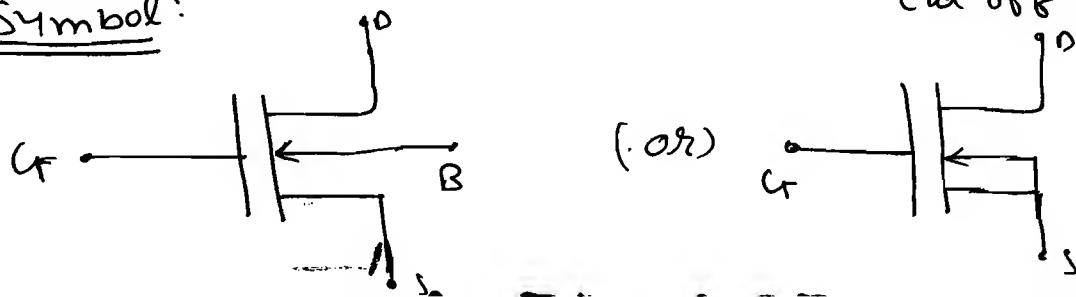
$V_{GDS} = -V$



* Output and Transfer Characteristics:



* Symbol:



⇒ Important Points to be Remember:

⇒ Pinch-off Voltage is -ve for n-channel DMOSFET.

⇒ n-channel Depletion MOSFET operates in enhancement mode for V_{GS} value and it operates in depletion mode for -ve V_{GS} value.

⇒ Depletion MOSFET operates in depletion and enhancement mode.

⇒ In discrete n-channel DMOSFET Substrate (or) Body (or) Bulk is connected to the ground (or) Source terminal. Whereas in IC's it should be connected to Most -ve voltage.

⇒ n-channel depletion MOSFET will be on for +ve V_{GS} value and it will be off for -ve V_{GS} value (i.e. $V_{GS} \leq V_p$).

⇒ Condition for Pinch-off (or) ~~break~~ Sat. is

$$V_{DS} = V_{GS} - V_p$$

\uparrow \uparrow \uparrow
 +ve +ve (or) -ve

⇒ Transfer characteristics of a depletion MOSFET gives pinch-off voltage (V_p), I_{DS} and transconductance g_m .

⇒ For $V_{GS} \leq V_p$ operates in Cut-off region and its drain current $I_D = 0$.

⇒ For $V_{GS} < V_{GS} - V_p$ it operates in linear region and its drain current

$$I_D = K_n \left[2(V_{GS} - V_p)V_{DS} - V_{DS}^2 \right]$$

$$K_n = \text{Constant} = \frac{I_{DSS}}{V_p^2} A l v^2$$

$$\therefore I_D = \frac{2I_{DSS}}{V_p^2} \left[(V_{GS} - V_p)V_{DS} - \frac{1}{2}V_{DS}^2 \right]$$

$\uparrow \quad \uparrow \quad \uparrow$
 (+ve or -ve +ve
 -ve)

⇒ for $V_{DS} \geq (V_{GS} - V_p)$ it operates in Saturation region and its drain current

$$I_D = K_n [V_{GS} - V_p]^2, \quad K_n = \frac{I_{DSS}}{V_p^2} A l v^2$$

$$\therefore I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_p} \right]^2$$

$\uparrow \quad \uparrow$
 (+ve or -ve)

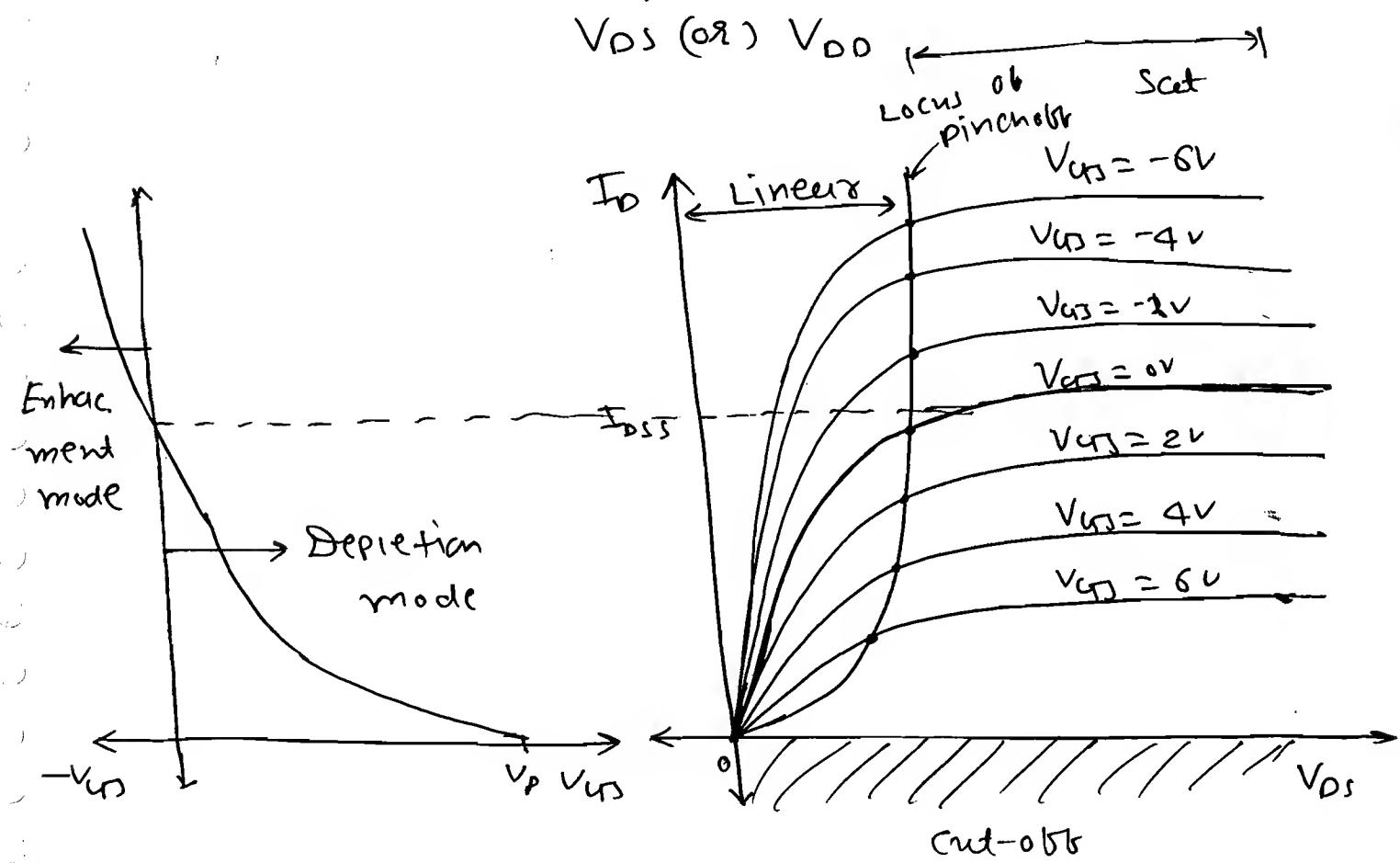
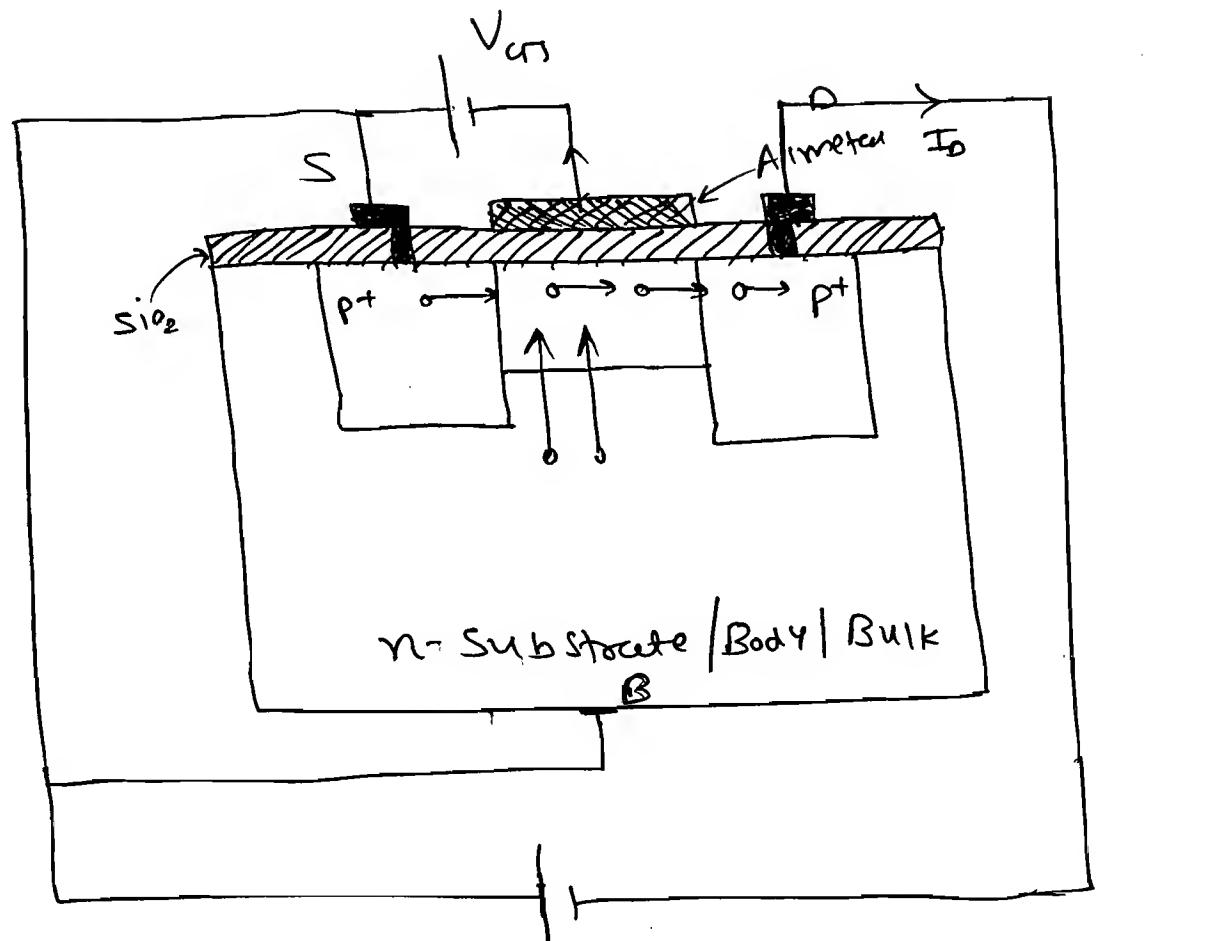


P- Channel

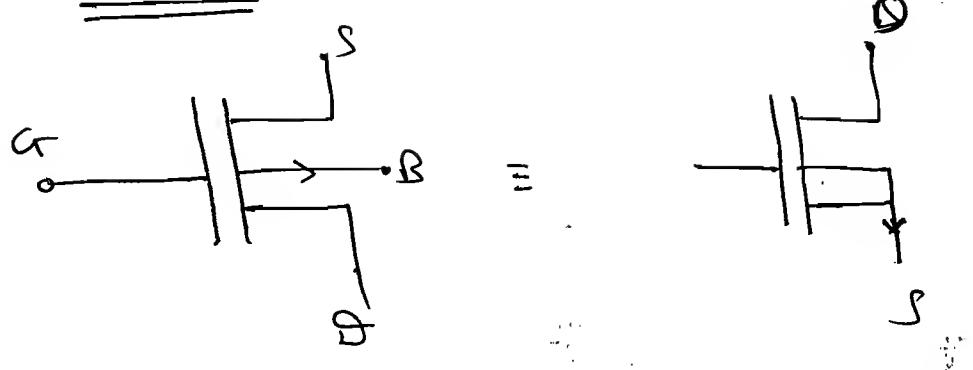
Depletion

MOSFET:

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* Symbol:



* Imp. points to be remember:

- ⇒ P-Channel depletion MOSFET operates with +ve as well as -ve V_{GS} value.
- ⇒ Pinch-off Voltage is +ve for P-DMOSFET
- ⇒ P-Channel depletion MOSFET operates in depletion mode for $+V_{GS}$ and it operates in enhancement mode for $-V_{GS}$ value.
- ⇒ In discrete P-DMOSFET Substrate (or) Body (or) Bulk should be connected to the ground (or) source terminal. Whereas in IC's it should be connected to the most +ve voltage.
- ⇒ P-DMOSFET will be ON for -ve V_{GS} values and it will be OFF for +ve values (i.e. $V_{GS} \geq V_P$).
- ⇒ Condition for pinch-off (or) Saturation

$$-ve \rightarrow V_{GS} = V_{GS} - V_P \leftarrow +ve$$

\Rightarrow For $V_{GS} \geq V_P$ P-DMOSFET operates in 4) cut-off region and its drain current $I_D = 0$.

\Rightarrow For $V_{DS} > V_{GS} - V_P$ it operates in linear region and its drain current is given by,

$$I_D = K_P \left[2(V_{GS} - V_P) \frac{V_{DS}}{V_P} - V_{DS}^2 \right].$$

$$K_P = \frac{I_{DSS}}{V_P^2}.$$

$$\therefore I_D = \frac{2 I_{DSS}}{V_P^2} \left[(V_{GS} - V_P) V_{DS} - \frac{1}{2} V_{DS}^2 \right].$$

+ve (or) +ve +ve
 -ve

$\Rightarrow V_{DS} \leq V_{GS} - V_P$ it operates in Saturation region and drain current,

$$I_D = K_P [V_{GS} - V_P]^2.$$

$$\therefore I_D = \frac{I_{DSS}}{V_P^2} [V_{GS} - V_P]^2.$$

$$\therefore I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2.$$

+ve (or) -ve
 +ve.

\Rightarrow We prefer D-MOSFET for resistor instead of E-MOSFET.

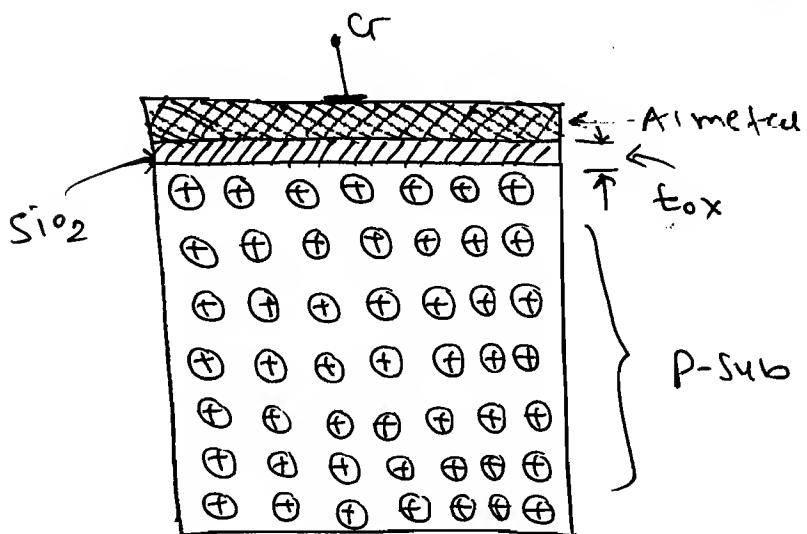
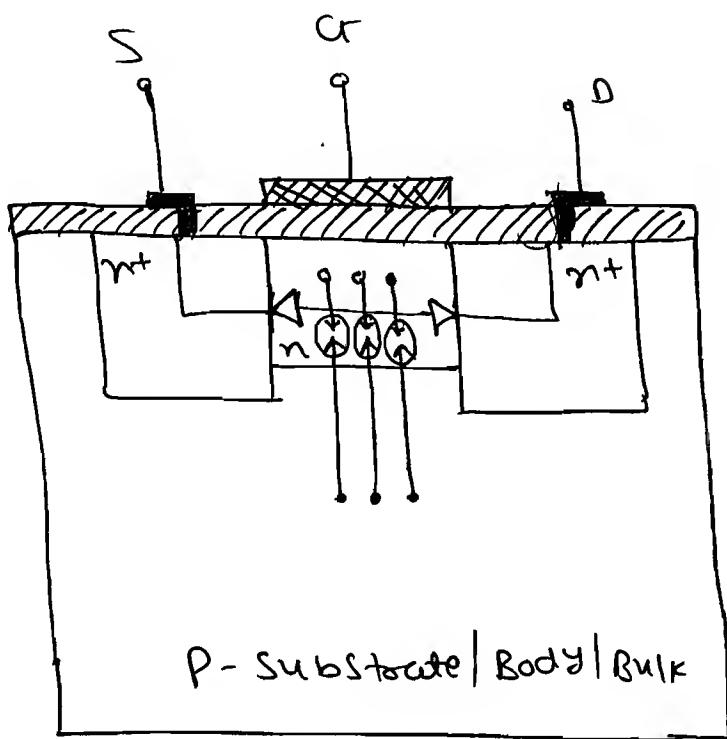
★ Enhancement

MosFET:

① n- Channel enhancement

MosFET: (n- EMosFET)

⇒



⇒

$$C = \frac{\epsilon A}{d}$$

$$C = \frac{\epsilon A_1}{d}$$

$$\& C = \frac{\epsilon A'}{d}$$

⇒ $\frac{C}{A} = \epsilon / d$ F/cm^2 (Q&) F/m^2 .

$$\therefore \frac{C}{A} = \epsilon_0 \cdot F/cm^2 \text{ (or) } F/m^2.$$

48)

$A = \text{Common Area bet^n two plate.}$

$\therefore C_{ox} = \text{oxide Capacitor per two unit area}$

$$\therefore C_{ox} = \frac{\epsilon_0}{t_{ox}}.$$

$$\therefore C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}. \quad F/cm^2 \text{ (or) } F/m^2.$$

$\Rightarrow t_{ox}$: Gate oxide thickness

ϵ_{ox} : Permittivity of SiO_2

$\epsilon_{ox} = \epsilon_{\text{sox}} \cdot \epsilon_0$, $\epsilon_{\text{sox}} = \text{relative permittivity of } \text{SiO}_2$

$$= 3.9 \approx 4$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$$

$$\epsilon_0 = 8.85 \times 10^{-14} \text{ F/cm.}$$

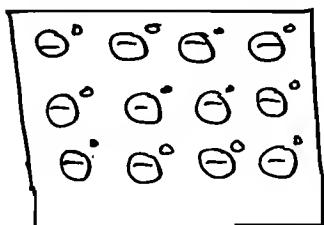
$$\therefore C_o = C_{ox} \cdot A$$

$$\therefore C_o = C_{ox} \times WL \quad (\text{F})$$

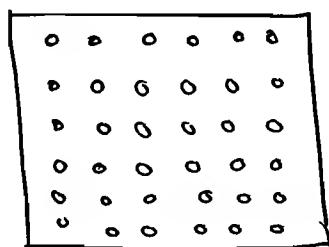
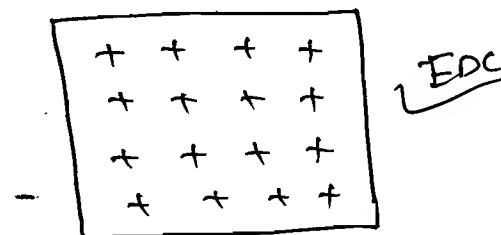
$C_o = \text{oxide Capacitance.}$

* P-type representation:

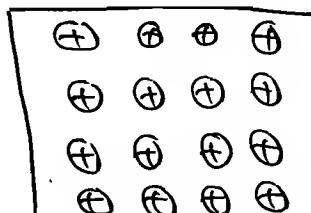
\Rightarrow



EDC



EDC

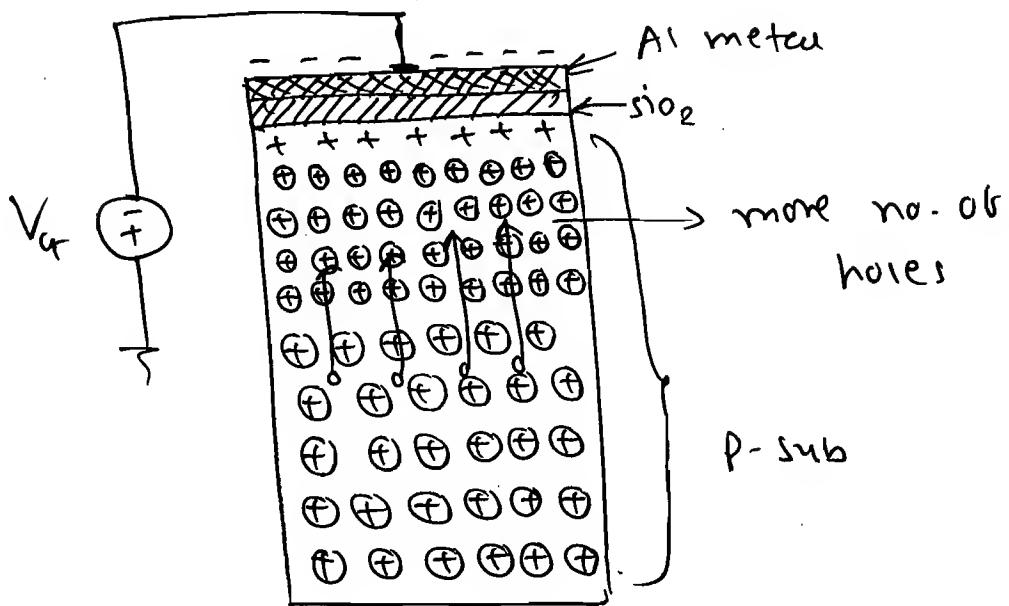


\oplus : hole

\ominus : electron

VLSI

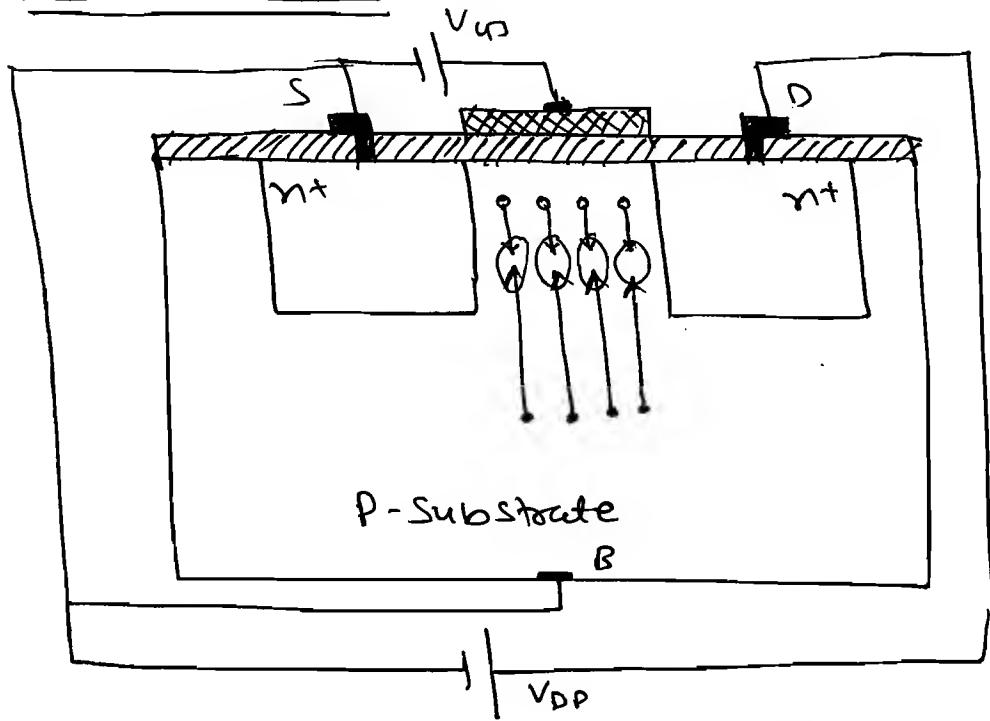
$$\Rightarrow V_{GDS} = -V_e$$



Accumulation mode.

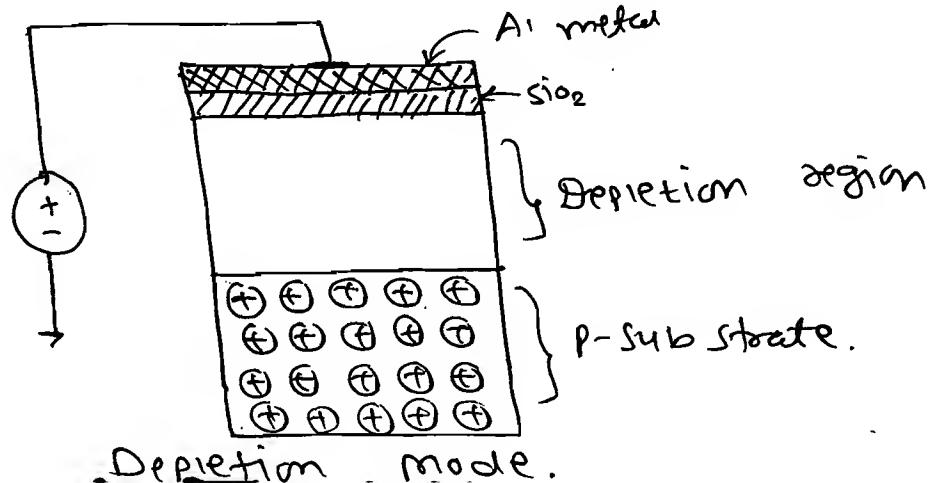
C_{ox} is same as that of for $V_{GDS} = 0V$.

$$\Rightarrow 0 < V_{GDS} < V_T:$$



$$C_{ox} = \frac{\epsilon_0}{d}$$

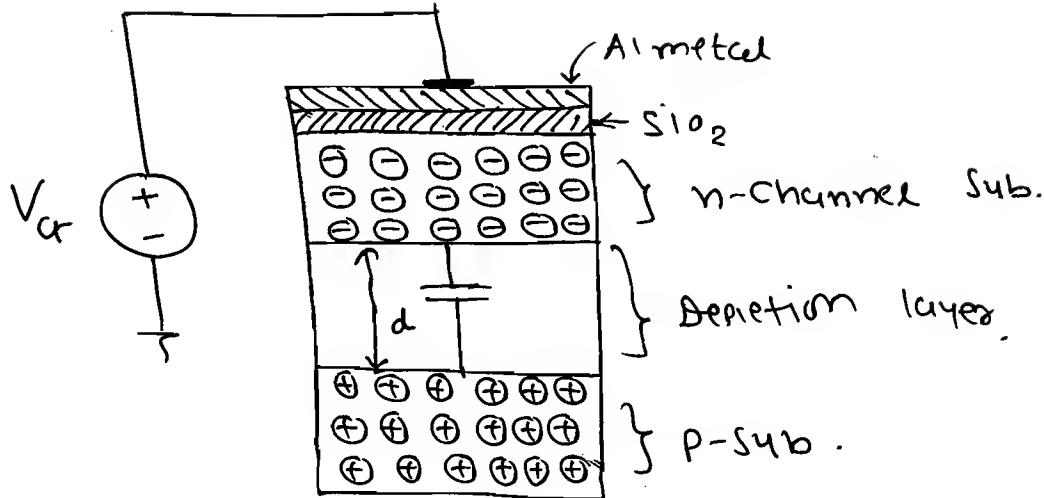
$C_{ox} \downarrow$ because $d \uparrow$



Depletion mode.

$$\textcircled{3} \quad \underline{V_{cr} > V_T}$$

\Rightarrow



(Inversion mode).

$$\Rightarrow R_{ox} = \frac{1}{C_{dep}}$$

C_{dep} : depletion Capacitance per unit area

$$C_{dep} = \frac{\epsilon_{Si} \cdot A}{d} \text{ F/cm}^2 \text{ (or) } \text{ F/m}^2$$

ϵ_{Si} : Permittivity of silicon Si.

d : Depletion layer thickness.

$$\epsilon_{Si} : \epsilon_{Si} \cdot \epsilon_0, \quad \epsilon_{Si} = 11.7 \approx 12$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m.}$$

$$\Rightarrow C_d = C_{dep} \cdot A = C_{dep} \cdot W \cdot L$$

C_d : depletion Capacitance.

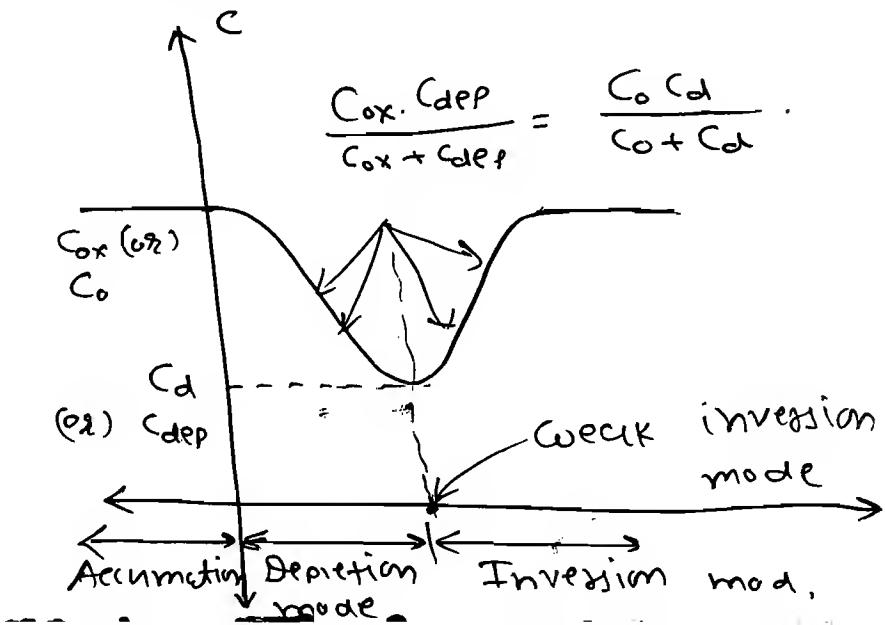
$$\Rightarrow C_{eq} = \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}}$$

$$\frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}} = \frac{C_o \cdot C_d}{C_o + C_d}$$

$$\therefore C_{eq} = \frac{C_o \cdot C_d}{C_o + C_d}$$

\Rightarrow if $t_{ox} \ll d$. [Imp.]

$$\Rightarrow \begin{cases} C_{ox} \gg C_{dep} \\ C_o \gg C_d \end{cases}$$



Q-22

CRQ

Page-48:

Here, ~~C_{ox}~~ $C_o = 7 \text{ PF}$

$$\therefore \text{C}_{ox} = \text{C}_o \quad \therefore C_o = \frac{\epsilon_0 \times A}{t_{ox}}$$

$$\therefore t_{ox} = \frac{3 \cdot 5 \times 10^{-3} \times 10^{-4}}{7 \times 10^{-12}}$$

$$t_{ox} = 0.5 \times 10^{-5} \times 10^{-2} \text{ cm}$$

$$\therefore t_{ox} = 0.5 \times 10^{-5} \times 10^{-2}$$

$$t_{ox} = 50 \text{ nm}$$

$$\Rightarrow C_{eq} = \frac{C_d \cdot C_{ox}}{C_d + C_{ox}}$$

$$C_d = \frac{\epsilon_s i \cdot A}{t_{ox} \cdot d}$$

$$\therefore I = \frac{C_d \times 7}{C_d + 7}$$

$$\therefore d = \frac{1 \times 10^{-12} \times 10^{-4}}{7 \times 10^{-12}} \times 6$$

$$\therefore C_d + 7 = 7 C_d$$

$$\therefore d = 0.143 \times 10^{-4} \text{ cm}$$

$$\therefore C_d = 7/16 \text{ PF}$$

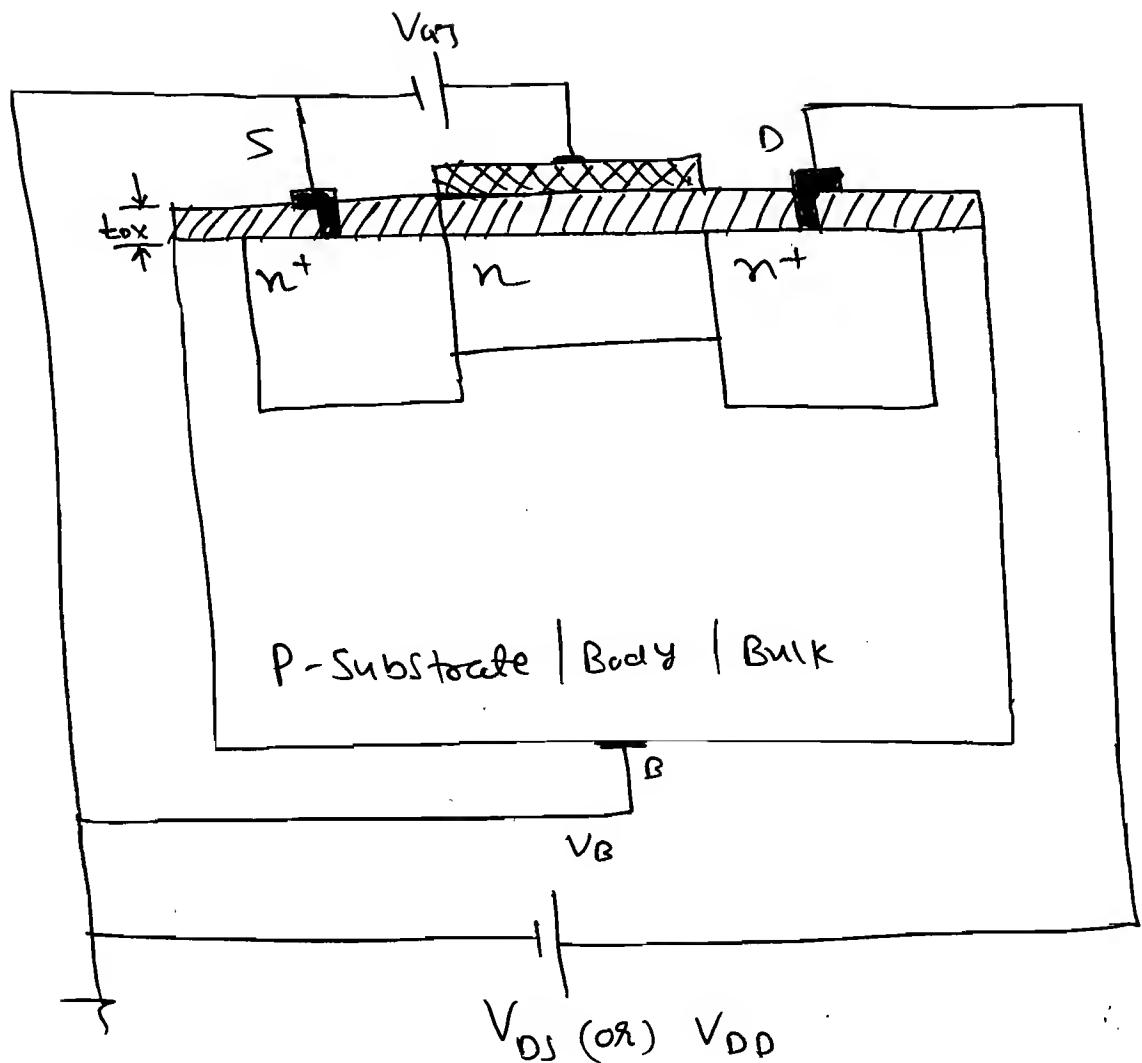
$$\therefore d = 0.143 \mu\text{m}$$

* Threshold

Voltage: (V_T):

\Rightarrow Threshold voltage is the minimum gate to source voltage required to accumulate sufficient no. of carriers and to form a channel betⁿ source and drain under the gate.

⇒



⇒ t_{ox} : Gate oxide thickness.

V_{SB} : Source to body voltage.

$N_A \text{ (or) } N_D$: Substrate doping density (or) concentration.

⇒ Threshold Voltage depends on

- Gate oxide thickness (t_{ox}).

- Source to body voltage (V_{SB}).

- Substrate doping density (or) concentration (N_A or N_D).

→ $V_t = f(t_{ox}, V_{SB}, N_A \text{ (or) } N_D)$.

⇒ Threshold Voltage of a MOSFET is increases w/ gate oxide thickness

increases (or) it decreases as t_{ox} decreases.

$$\rightarrow t_{ox} \uparrow \rightarrow V_T \uparrow$$

$$t_{ox} \downarrow \rightarrow V_T \downarrow.$$

\Rightarrow Threshold Voltage of a MOSFET is decreases as Source to Body voltage decreases. (or) it increases with increase in V_{SB} .

$$\Rightarrow V_{SB} \uparrow \rightarrow V_T \uparrow$$

$$V_{SB} \downarrow \rightarrow V_T \downarrow.$$

\Rightarrow Threshold voltage of a MOSFET increases as increases in doping density increases. (or) it decreases as substrate doping density decreases.

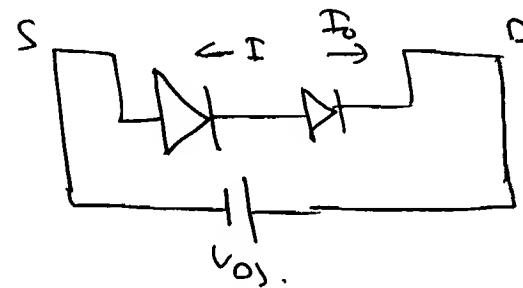
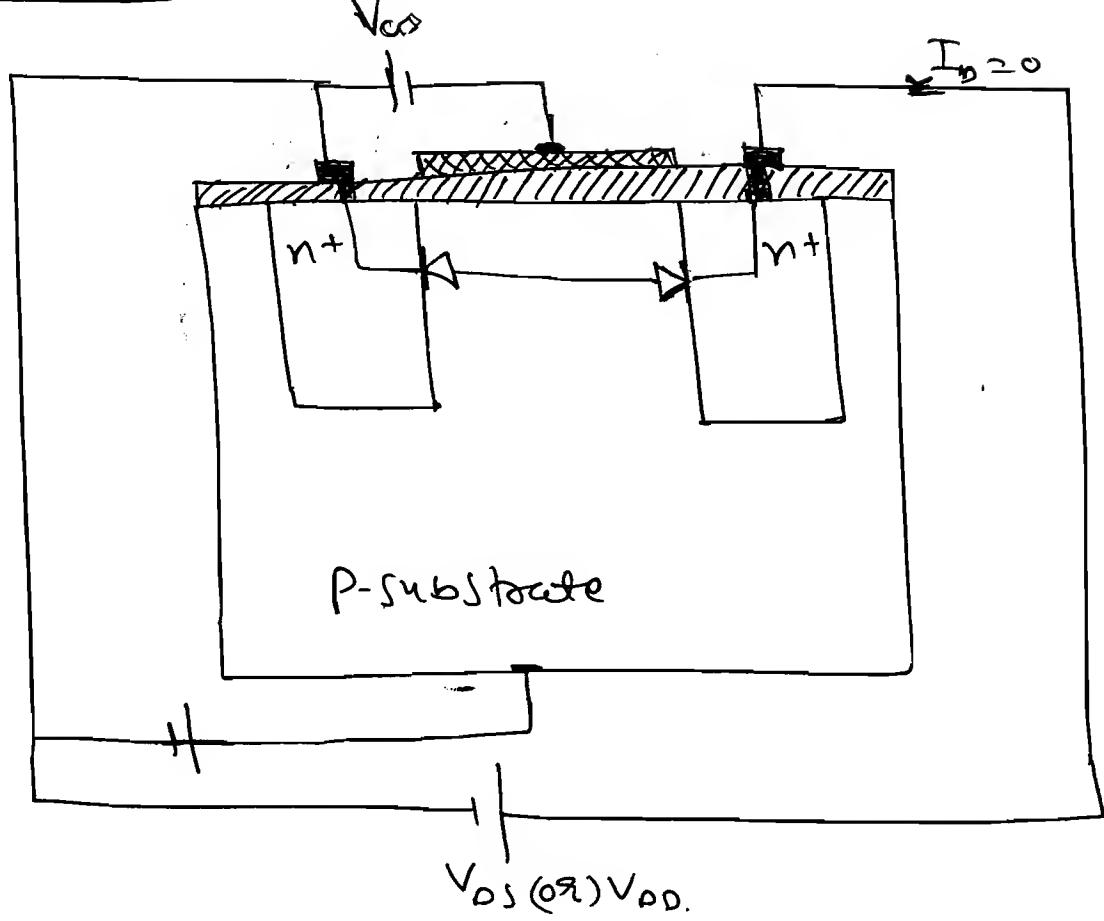
$$N_A \text{ (or) } N_D \uparrow \rightarrow V_T \uparrow$$

$$N_A \text{ (or) } N_D \downarrow \rightarrow V_T \downarrow.$$

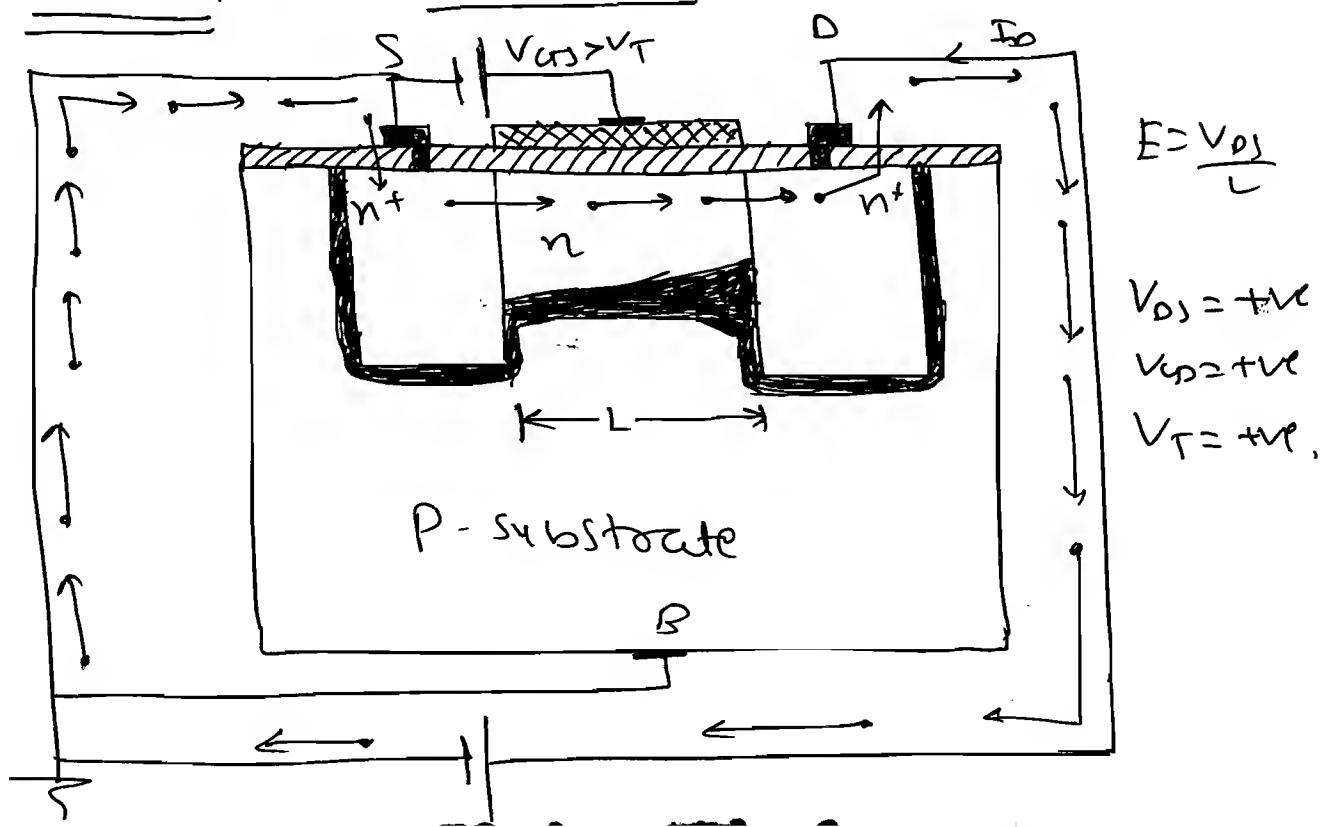
\Rightarrow Threshold Voltage is +ve for n-channel enhancement MOSFET and it is -ve for p-channel.

① $V_{GDS} < V_T$: (cut-off).

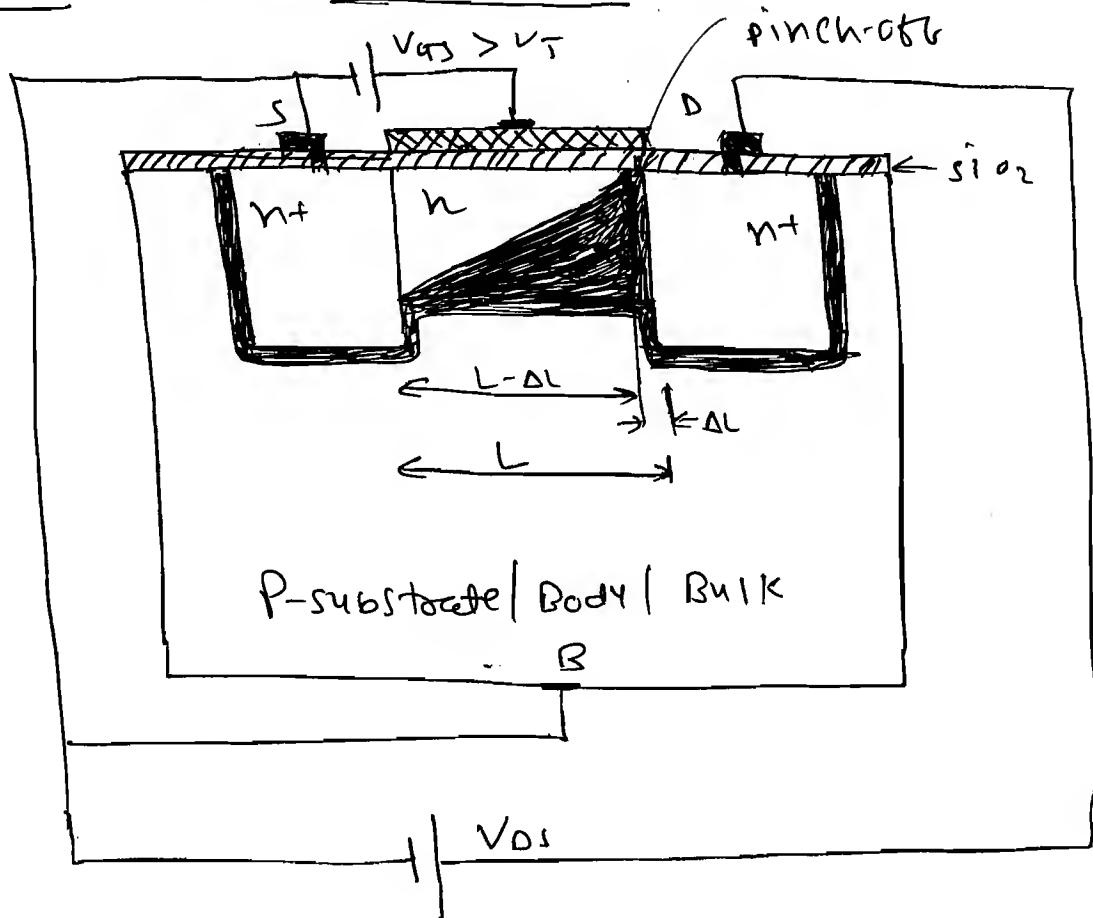
51)



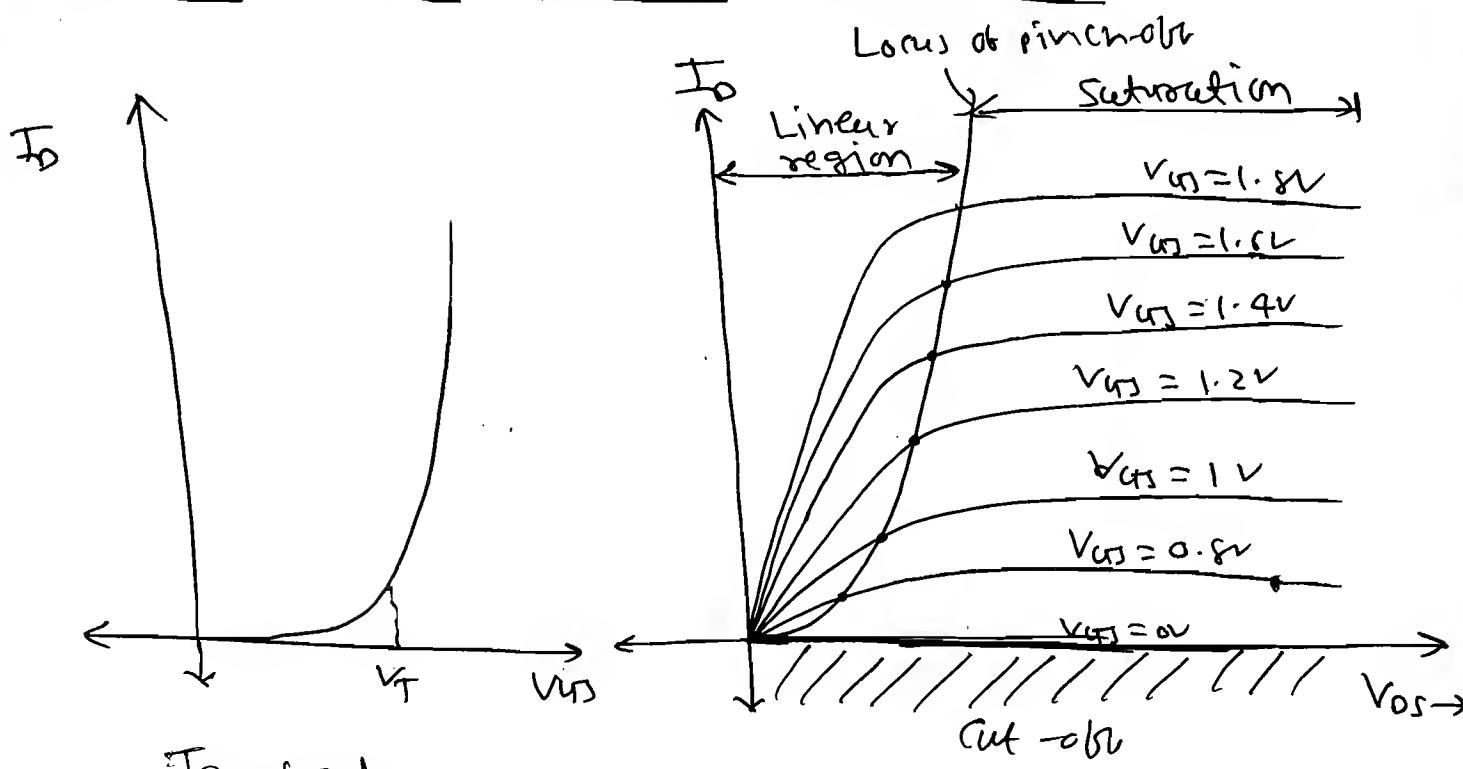
(ii) $V_{GDS} > V_T$ & $V_{DS} < V_{GS} - V_T$: (Linear):



$$(iii) \underline{V_{GDS} > V_T} \quad \underline{\Rightarrow} \quad \underline{V_{DS} > V_{GS} - V_T} \quad (\text{saturation})$$



* Drain and transfer Characteristics:



(Drain Characteristics)

⇒ From drain characteristics,

we can only V_T & g_m be extracted.

52) \Rightarrow Channel Conductivity $\propto (V_{GS} - V_T)$.

\Rightarrow Drain Current (I_D) $\propto (V_{GS} - V_T)$.

\Rightarrow

$$V_{DS} = V_{GS} - V_T$$

+ve +ve +ve

$V_{DS} < V_{GS} - V_T$: Linear

$V_{DS} > V_{GS} - V_T$: Saturation.

\Rightarrow $V_T, V_{GS} \& V_{DS}$:

\rightarrow if $V_{GS} < V_T$: Cut-off

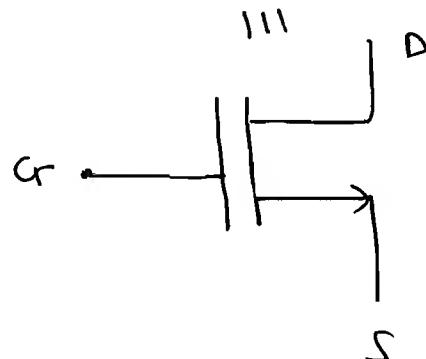
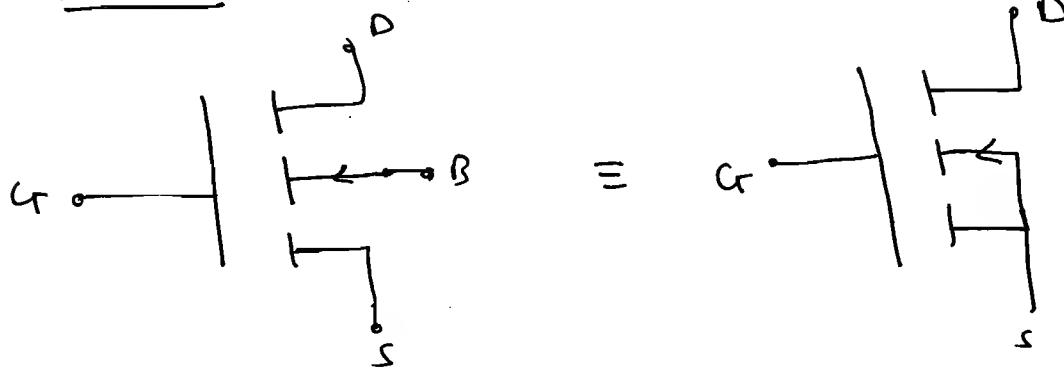
\rightarrow if $V_{GS} > V_T$

Calculate $V_{GS} - V_T$.

• if $V_{DS} < V_{GS} - V_T$: Linear

• if $V_{DS} \geq V_{GS} - V_T$: Saturation.

\Rightarrow Symbol:



* Important Points to be remembered:

⇒ n- Channel E- MOSFET operates with +ve gate voltages i.e. +ve V_{GS} values.

⇒ Gate to Source Voltage (V_{GS}) and Threshold Voltage (V_T) are the for n channel enhancement mosFET.

⇒ n- EMOSFET operate in enhancement mode for +ve V_{GS} values.

⇒ n- EMOSFET always operates in enhancement mode.

⇒ In discrete n- Channel EMOSFET, Substrate (or) Body is connected to the ground or source terminal whereas in IC's it should be connected to the most -ve voltage.

⇒ n- channel EMOSFET will be on for + V_{GS} values (i.e. $V_{GS} > V_T$) and it will be off for 0 (or) -ve V_{GS} values. (i.e. $V_{GS} < V_T$).

⇒ At a given V_{GS} i.e. ($V_{GS} > V_T$) as drain to source voltage increases the width of the drain depletion region increases.

→ At a particular value of V_{DS} , the thickness of the channel near to drain becomes zero it is called pinch-off. 53)

⇒ Condition for the pinch-off (or) Sat is $V_{DS} = V_{GS} - V_T$. Here, all are +ve.

⇒ The Potential (or) Voltage across the Channel increases from source to drain end, therefore the R.B. b/w channel and substrate increases from source to drain end.

⇒ The width of the depletion region betⁿ channel and substrate increases from source to drain end. Therefore the thickness of the channel decreases from source to drain end.

⇒ The inversion charge across the channel decreases from source to drain end.

⇒ At pinch-off (or) Saturation the channel is in flattered shape.

⇒ The electric field across the channel remains constant at pinch off (or) Saturation.

⇒ Linear region also called by Ohmic region
(or) triode region.

⇒ Linear region is the region left side to the pinch-off Locus.

⇒ Saturation region is the region right side to the locus of pinch-off.

⇒ Cut-off region is the region below the $V_{DS} < V_T$.

⇒ MOSFET can be operate as an Amplifier in Saturation and it can be operate as a switch in Linear and Cut-off region.

⇒ MOSFET can be used as a Voltage Variable Resistor in linear region and it can be used as a current source in the saturation region.

⇒ Transfer Characteristic of a F-MOSFET gives V_T & g_m .

⇒ For $V_{GS} < V_T$, n- EMOSFET operates in Cut-off region and it drain current $I_D = 0$ A.

⇒ For $V_{GS} > V_T$ & $V_{DS} < V_{GS} - V_T$ it operates in linear region and it drain current I_D is,

$$\Rightarrow I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right].$$

54)

\uparrow +ve \uparrow +ve \uparrow +ve

→ C_{ox} : Oxide Capacitance per unit area.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}.$$

t_{ox} : Gate oxide thickness.

ϵ_{ox} : Permittivity of SiO_2 .

$$\epsilon_{\text{d}ox} = 3.9 \approx 4$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m.}$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/cm.}$$

⇒ For $V_{GS} > V_T$ & $V_{DS} \geq (V_{GS} - V_T)$ it
operates in Sat. region and its drain
current.

$$I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} \left[(V_{GS} - V_T) \right]^2$$

\uparrow +ve \uparrow +ve

(Q) - An n-channel enhancement MOSFET has $V_T = 0.7 \text{ V}$, and $V_{GS} = 1.5 \text{ V}$. Find the region of operation for $V_{DS} = 2.5 \text{ V}$.

Soln: Here, $V_T = 0.7 \text{ V}$, $V_{GS} = 1.5 \text{ V}$.

$$V_{DS} = 2.5$$

$$\therefore V_{GS} > V_T$$

$$\text{and } V_{GS} - V_T = 1.5 - 0.7 = 0.8 \text{ V}$$

$$\therefore V_{DS} > (V_{GS} - V_T = 0.8 \text{ V})$$

So, in Saturation.

(Q) - n-channel enhancement MOSFET has $V_T = 0.7 \text{ V}$ and $V_{GS} = 3 \text{ V}$. Find the region of operation for $V_{DS} = 2 \text{ V}$.

Soln: $V_{GS} = 3 \text{ V}$, $V_T = 0.7 \text{ V}$

$$V_{GS} > V_T$$

$$\& V_{GS} - V_T = 3 - 0.7 = 2.3 \text{ V}$$

$$(V_{DS} = 2 \text{ V}) < (V_{GS} - V_T = 2.3 \text{ V})$$

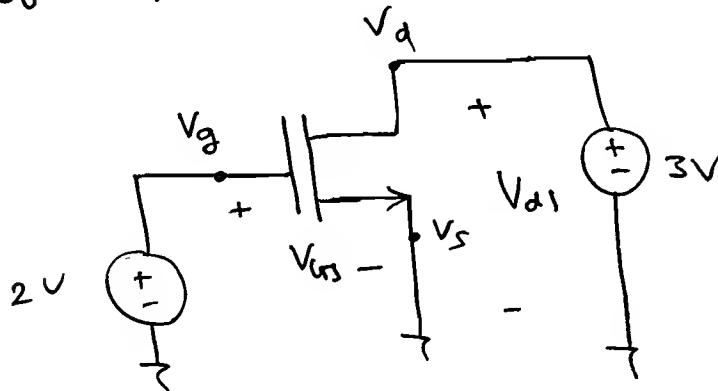
So, it operates in linear region.

(Q) : n-EMOSFET has $V_{GS} = 1.2 \text{ V}$ & $V_T = 1.5 \text{ V}$. Find region of operation for $V_{DS} = 4 \text{ V}$.

Soln: $V_{GS} = 1.2 \text{ V}$, $V_T = 1.5 \text{ V}$

$V_{GS} < V_T \Rightarrow$ it operates in cut-off region.

Q For the CKT shown in the figure. MOSFET has threshold voltage $0.6V$. Find the region of operation.



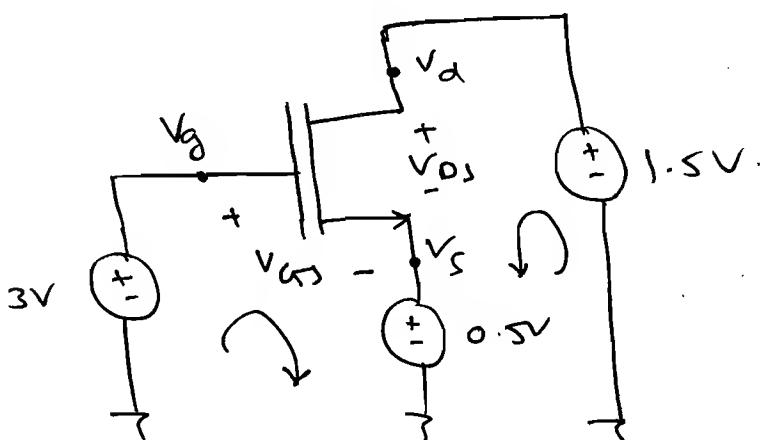
Solⁿ: By KVL $2 - V_{GS} = 0 \Rightarrow V_{GS} = 2V$ $V_{DS} - 3 = 0 \Rightarrow V_{DS} = 3V$

$V_T = 0.6V$ $V_{GS} > V_T \Rightarrow V_{GS} - V_T = 2 - 0.6 = 1.4$

$\therefore V_{DS} > (V_{GS} - V_T = 1.4)$

so, it operates in saturation.

Q For the CKT shown in the fig. MOSFET has $V_T = 0.6$. Find the region of operation.



Solⁿ: By KVL, $3 - V_{GS} - 0.5 = 0 \Rightarrow V_{GS} = 2.5V$

By KVL, $1.5 - V_{DS} - 0.5 = 0$

$\Rightarrow V_{DS} = 1V$

$\& V_T = 0.6$
(given).

$$\text{Now, } V_{DS} = 2.5 > (V_T = 0.6V)$$

$$V_{DS} - V_T = 2.5 - 0.6 = 1.9V$$

$$\therefore (V_{DS} = 1) < (V_{DS} - V_T) = 1.9$$

Therefore, it operates in linear region.

* Imp:

① Linear:

$$\Rightarrow I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \left[(V_{DS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right].$$

$$\Rightarrow I_D = K_n' \cdot \frac{W}{L} \left[(V_{DS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$\text{where, } K_n' = \mu_n \cdot C_{ox} \cdot (A1V^2).$$

$$K_n' = \frac{I_D}{(V_{DS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2} \cdot (A1V^2).$$

$$\Rightarrow I_D = \beta_n \left[(V_{DS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$\beta_n = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot A1V^2$$

$$\beta_n = K_n' \cdot \frac{W}{L} \cdot A1V^2.$$

$$\Rightarrow K_n' = K', \quad \beta_n = \beta. = K.$$

② Saturation:

$$\Rightarrow I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} [V_{DS} - V_T]^2.$$

$$I_D = \frac{1}{2} \cdot K_n' \cdot \frac{W}{L} [V_{DS} - V_T]^2.$$

$$\Rightarrow I_D = K_n [V_{DS} - V_T]^2.$$

$$K_n = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (A1V^2).$$

$$K_n = \frac{1}{2} K_n' \cdot \frac{W}{L} \cdot (A1V^2).$$

$$I_D = \frac{1}{2} \beta_n [V_{DS} - V_T]^2, \quad \beta_n = \mu_n C_{ox} \cdot \frac{W}{L} \quad (V/m^2)$$

* Deep Triode Region:

\Rightarrow Deep triode region is also a linear region but for small values of V_{DS} .

\Rightarrow Condition for Deep Triode Region is,

$$\therefore V_{DS} \ll 2 [V_{DS} - V_T].$$

$$\Rightarrow I_D = \mu_n C_{ox} \cdot \frac{W}{L} \cdot \left[[V_{DS} - V_T] V_{DS} - \frac{1}{2} V_{DS}^2 \right].$$

in linear region.

for deep triode region it is given by.

$$I_D = \mu_n C_{ox} \cdot \frac{W}{L} \times [(V_{DS} - V_T) V_{DS}].$$

$$I_D = K_n' \cdot \frac{W}{L} \times (V_{DS} - V_T) \cdot V_{DS}.$$

$$I_D = \beta_n (V_{DS} - V_T) V_{DS}. \quad K_n' = \mu_n C_{ox}.$$

$$\beta_n = \mu_n C_{ox} \times \frac{W}{L} = K_n' \cdot \frac{W}{L}.$$

$$\begin{aligned} K_n &= K = \beta_n \\ &= K_n' \cdot \frac{W}{L} \\ &= \mu_n C_{ox} \cdot \frac{W}{L}. \end{aligned}$$

* Drain ON Resistance (or) ON resistance
(or) Drain to Source resistance.

$\Rightarrow \gamma_{ds(on)}$, $\gamma_{dc(on)}$, R_{on} .

\Rightarrow Pinch-off point in drain characteristic
 of MOSFET is \Rightarrow called V_{ds} (or) V_{dmin} (or)
 V_{sat} (or) over drive Voltage

$$V_{ov} = V_{ds} - V_T.$$

\Rightarrow It is the resistance offered by the MOSFET in the linear region for small values of V_{ds} .

\Rightarrow It is the reciprocal of the slope of the drain characteristic in the linear region for small value of V_{ds} .

$$\gamma_{ds(on)} = \gamma_{dc(on)} = R_{on} = \frac{1}{\frac{\Delta I_D}{\Delta V_{ds}}}$$

$$\therefore R_{on} = \frac{\Delta V_{ds}}{\Delta I_D} \Big|_{V_{ds}}$$

$$R_{on} = \frac{dV_{ds}}{dI_D} \Big|_{V_{ds}}$$

$$\Rightarrow I_D = M_n \cdot C_{ox} \cdot \frac{W}{L} [V_{ds} - V_T] V_{ds}.$$

$$\therefore \frac{dI_D}{dV_{ds}} = M_n \cdot C_{ox} \cdot \frac{W}{L} (V_{ds} - V_T).$$

$$\begin{aligned}
 \therefore R_{on} &= \gamma_{d(\text{con})} = \gamma_{d(\text{scn})} = \frac{1}{\text{Mn. Cox.} \cdot \frac{w}{L} (V_{GS} - V_T)} \quad (57) \\
 &= \frac{1}{K_n \cdot \frac{w}{L} (V_{GS} - V_T)} \\
 &= \frac{1}{B_n \cdot (V_{GS} - V_T)} \\
 \therefore R_{on} &\propto \frac{1}{(w/L)} \\
 C &\propto \frac{w}{L}.
 \end{aligned}$$

$(V_{GS} - V_T) \leftarrow V_{ov}$
overdrive voltage

* Trans Conductance

(g_m) :

⇒ Trans Conductance is also called as mutual conductance (or) Figure of merit.

⇒ It gives how effectively MOSFET converts the voltage changes at input to the corresponding current changes at the output in saturation region.

⇒ Trans Conductance is also equal to the slope of the transfer characteristics.

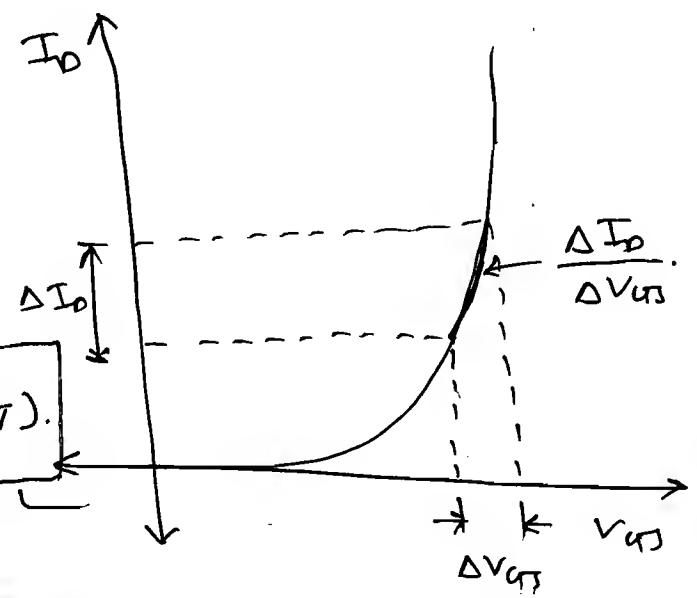
$$\Rightarrow I_D = \frac{1}{2} \text{Mn. Cox.} \cdot \frac{w}{L} [V_{GS} - V_T]^2.$$

$$\therefore \frac{dI_D}{dV_{GS}} = \text{Mn. Cox.} \cdot \frac{w}{L} [V_{GS} - V_T].$$

$$\therefore g_m = \frac{dI_D}{dV_{GS}} = \text{Mn. Cox.} \cdot \frac{w}{L} (V_{GS} - V_T).$$

$$\therefore g_m = \frac{1}{R_{on}}$$

- ①



$$\Rightarrow g_m = \sqrt{2 \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} - ②.$$

$$g_m \approx k_m (v_{GS} - v_T)$$

$$\Rightarrow g_m = \sqrt{2 \mu_n \cdot C_{ox} \cdot \frac{W}{L}} \cdot \sqrt{\frac{1}{2} \mu_n C_{ox} \cdot \frac{W}{L} \cdot (v_{GS} - v_T)^2}$$

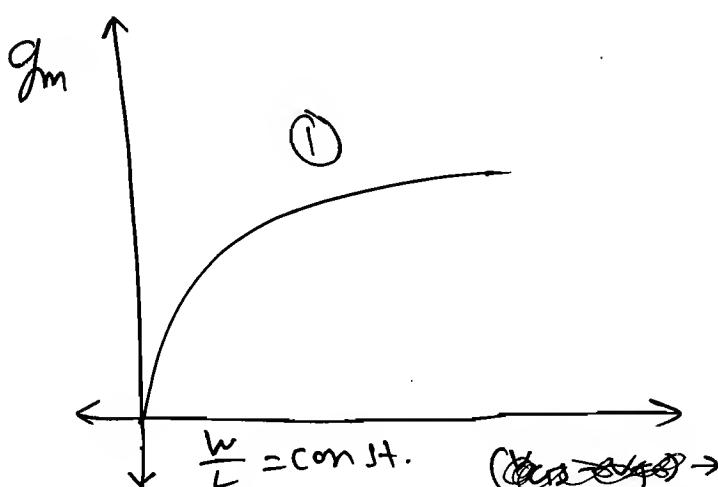
$$\therefore g_m = \sqrt{2 \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D} \quad (\text{AIV})$$

$$\Rightarrow g_m = \frac{2 I_D}{v_{GS} - v_T} - ③.$$

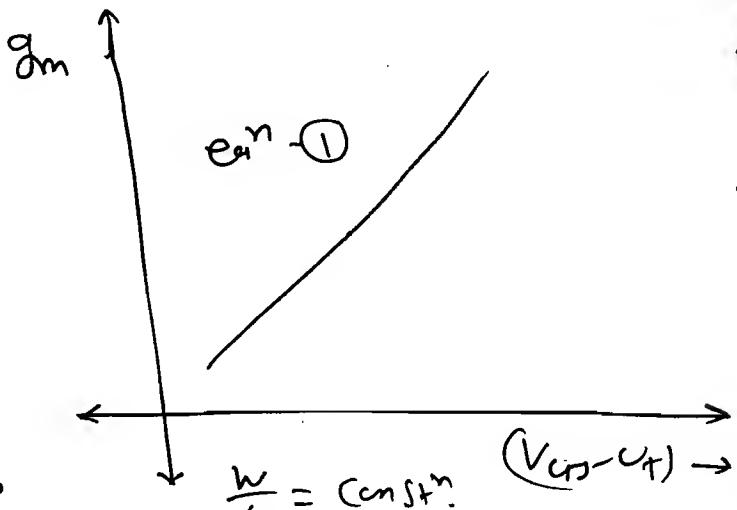
$$\rightarrow g_m = \frac{2 \cdot \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (v_{GS} - v_T)^2}{(v_{GS} - v_T)}$$

$$\therefore g_m = \frac{2 I_D}{v_{GS} - v_T}$$

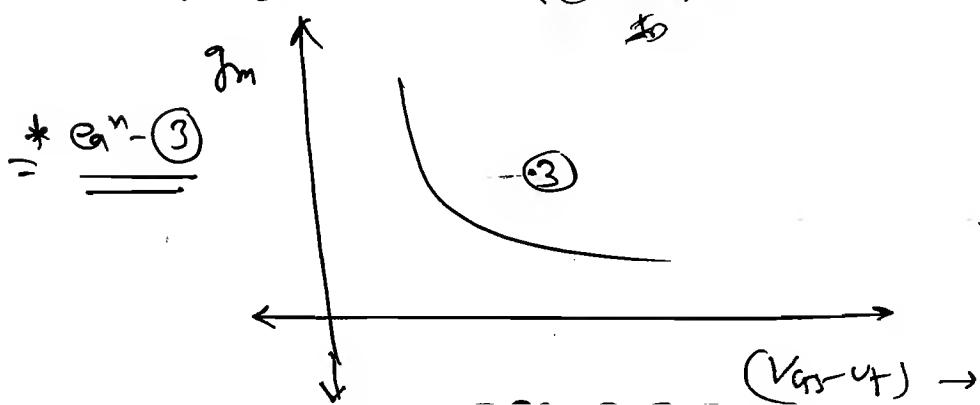
$$(*) \underline{\underline{g_m - ①}}$$



$$(*) \underline{\underline{g_m - ②}}$$



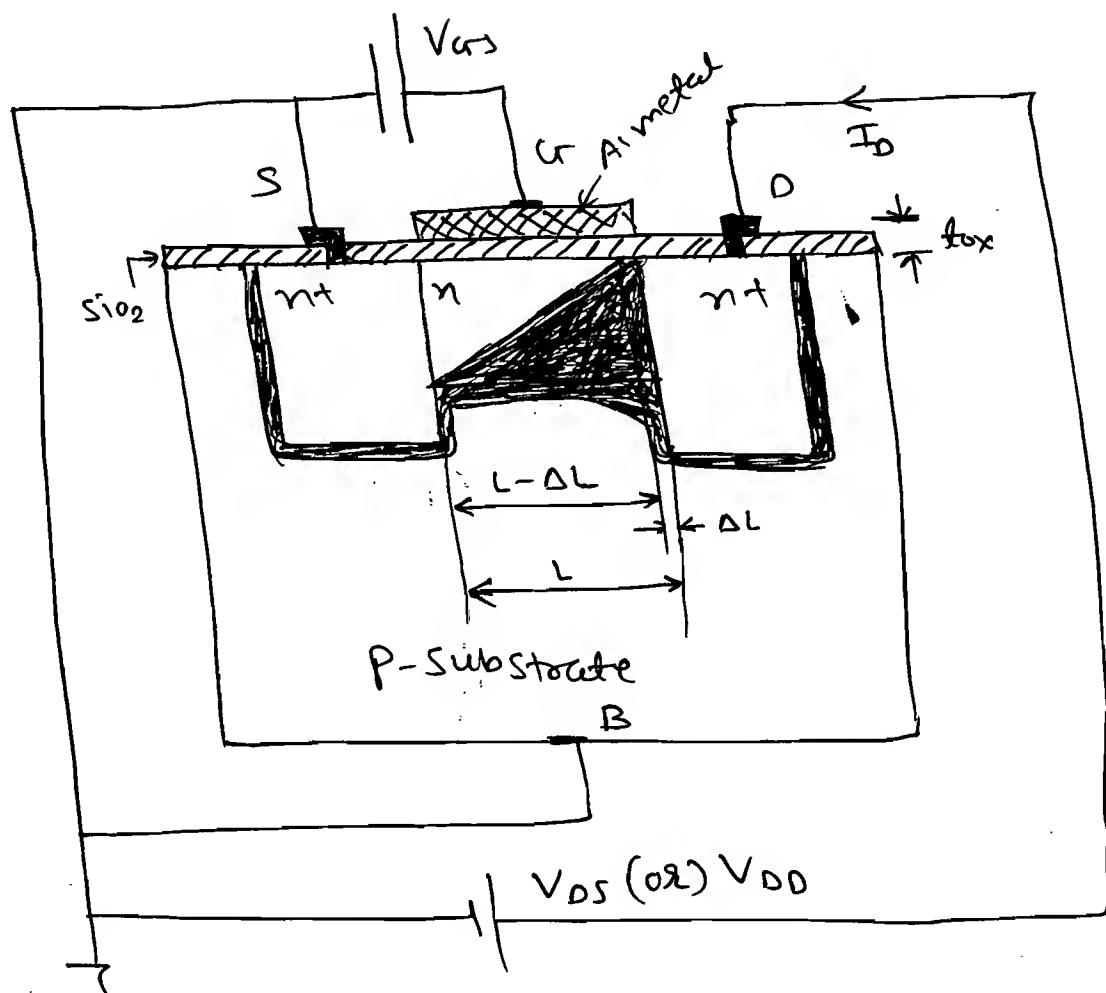
$$(*) \underline{\underline{g_m - ③}}$$



* Channel Length Modulation:

58)

⇒



⇒ In the saturation region as drain to source increases the effective length of the channel decreases i.e. as V_{DS} varies the length of the channel is varies it is called channel length modulation.

⇒ Due to channel length modulation drain current increases and it is given by

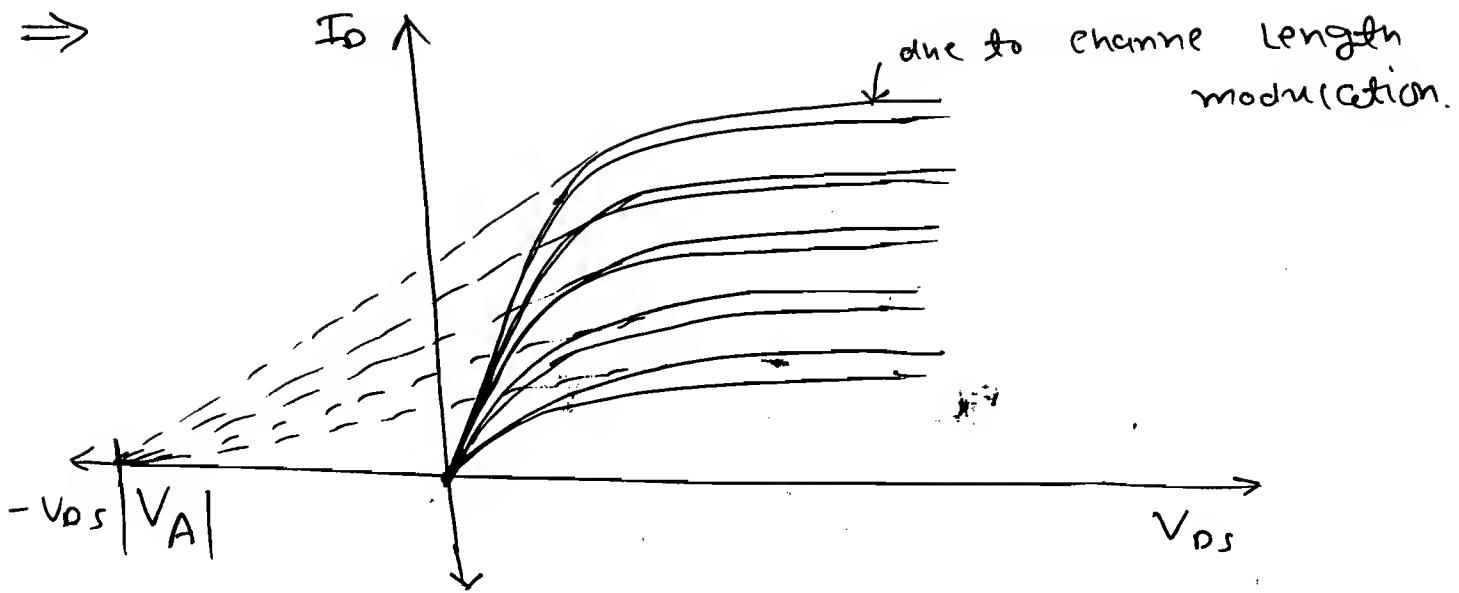
$$I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2 (1 + \lambda V_{DS}).$$

$$\lambda = \frac{1}{V_A} ; V_A = \text{Early Voltage.}$$

$$V_{DS} = V_{GS} - V_{DS} > V_T$$

or

$$V_{DS} = V_{GS} - V_{DS} = V_T$$



* Drain Resistance (or) Output Resistance :

γ_d (or) r_o :

⇒ It is the resistance offered by the MOSFET in the saturation region.

⇒ It is the reciprocal of the slope of drain characteristics in the saturation region.

$$\Rightarrow \text{Slope} = \left. \frac{\Delta I_D}{\Delta V_{DS}} \right|_{V_{DS}}$$

$$\gamma_d \text{ (or) } r_o = \left. \frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}} \right|_{V_{DS}} = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{DS}} = \left. \frac{\frac{\Delta V_{DS}}{\Delta I_D}}{\Delta V_{DS}} \right|_{V_{DS}} = \left. \frac{dV_{DS}}{dI_D} \right|_{V_{DS}}$$

$$\gamma_d \text{ (or) } r_o = \frac{1}{\lambda I_D}$$

$$\Rightarrow I_D = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} \left[(V_{DS} - V_T)^2 \right] (1 + \lambda V_{DS}).$$

$$\therefore \frac{dI_D}{dV_{DS}} = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} \left[(V_{DS} - V_T)^2 \right] \cdot \lambda.$$

I_D (without channel length modulation)

$$\therefore \frac{dI_D}{dV_{DS}} = \lambda \cdot I_D.$$

$$\therefore \gamma_{D(\text{or})} \gamma_0 = \frac{1}{\lambda I_D} = \frac{V_A}{I_D} \quad (\because \lambda = \frac{1}{V_A}).$$

\Rightarrow Drain resistance (or) OIP resistance is also called A.C. resistance (or) small signal resistance.

* Body effect:

\rightarrow due to body effect $V_T \uparrow$
 $\Rightarrow V_{SB}$: Source to Body Voltage.

V_{TO} : Threshold Voltage of MOSFET when $V_{SB} = 0$.

$$V_T = V_{TO} + \gamma \left[\sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s} \right].$$

V_T : Threshold voltage of MOSFET at a given V_{SB} .

ϕ_s : Surface potential, $\phi_s = 2V_T \ln \left(\frac{N_A}{n_i} \right)$.

V_T : Thermal voltage.

$$V_T: \frac{T}{11,600} = \frac{300}{11,600} = 0.02586 = 26 \text{ mV}.$$

γ : Body Effect Coefficient.

$$\gamma = \frac{\sqrt{2 \pi N_A \cdot \epsilon_{Si}}}{C_{ox}}, \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}.$$

$$\gamma = \frac{t_{ox}}{\epsilon_{ox}} \cdot \sqrt{2 \pi N_A \epsilon_{Si}}.$$

$$\Rightarrow t_{ox} \uparrow \rightarrow V_T \uparrow \quad | \quad V_{SB} \uparrow \rightarrow V_{SB} \uparrow \quad | \quad (N_A \text{ or } N_D) \uparrow \rightarrow V_T \uparrow$$

$$t_{ox} \downarrow \rightarrow V_T \downarrow \quad | \quad V_{SB} \downarrow \rightarrow V_{SB} \downarrow \quad | \quad (N_A \text{ or } N_D) \downarrow \rightarrow V_T \downarrow$$

\Rightarrow Due to body effect threshold voltage increases. Therefore drain current decreases.

* Temperature effect:

$$\Rightarrow V_T \propto k_n^{-1} = \ln C_{ox}$$

\Rightarrow Case - (i): V_T

V_T : dependent on Temperature.

V_T : dec by $2m \text{ } ^\circ\text{C}$.

$$T \uparrow \rightarrow V_T \downarrow \rightarrow I_o \uparrow$$

PTC

\Rightarrow Case - (ii):

$$\rightarrow k_n^{-1} = \ln C_{ox}$$

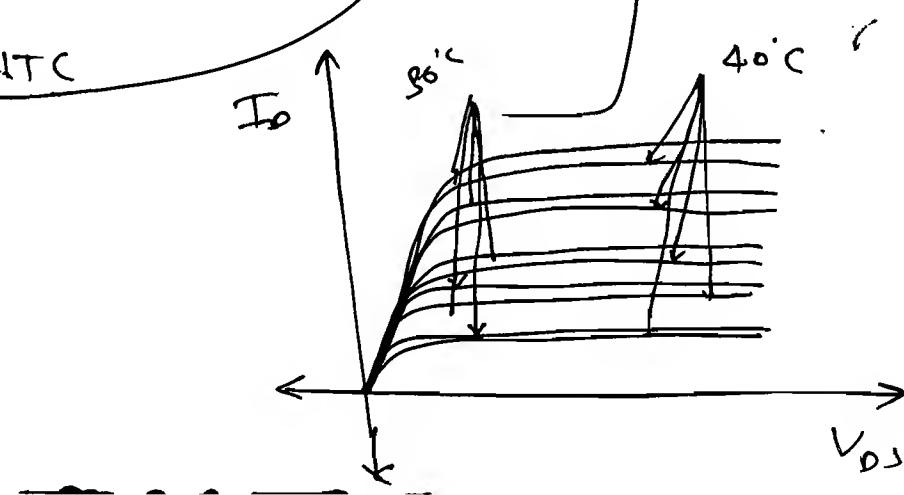
$$\ln n \propto \frac{1}{T^m} \Rightarrow \mu \propto T^{-m}$$

$$T \uparrow \rightarrow \mu_n \downarrow \rightarrow I_o \downarrow$$

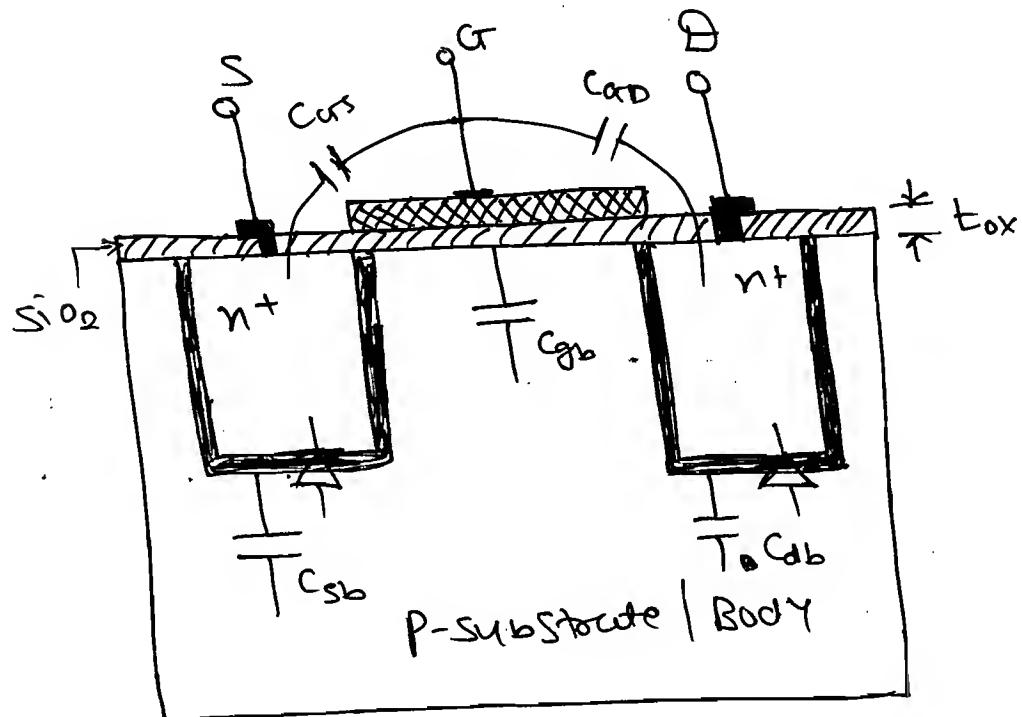
NTC

$$T \uparrow \rightarrow I_o \downarrow$$

NTC



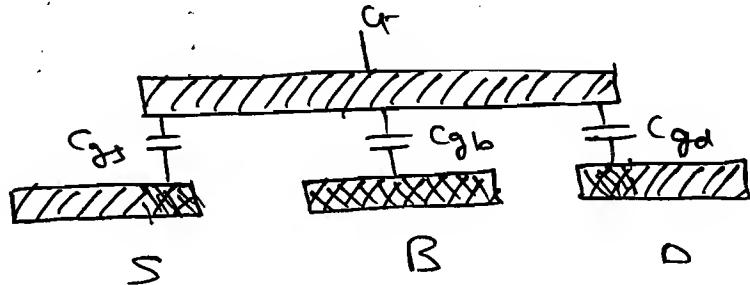
* Mos Capacitor: Imp: 60



① Gate Capacitors:

- (i) Gate to Source Cap. (C_{gs})
- (ii) Gate to drain Cap. (C_{gd}).
- (iii) Gate to body Cap. (C_{gb}).

⇒



$$C_g = C_{gs} + C_{gd} + C_{gb}.$$

C_g : Total gate Capacitance.

② junction Capacitors:

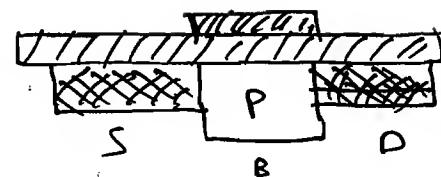
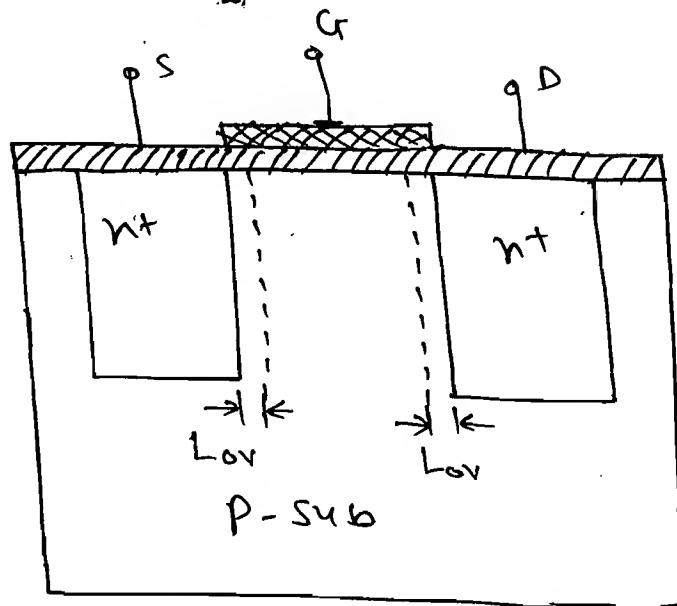
- (i) Source to body junction Cap. (C_{gb}).
- (ii) Drain to body junction Cap. (C_{db}).

1. Gate Capacitors:

$$\rightarrow C_{gs} = 0 + \text{Cox} \cdot W L_{ov} \cdot * \frac{\text{Cut-off}}{\text{Cut-off}}$$

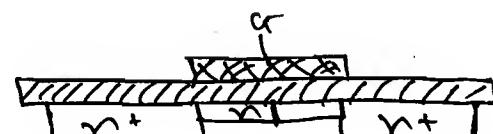
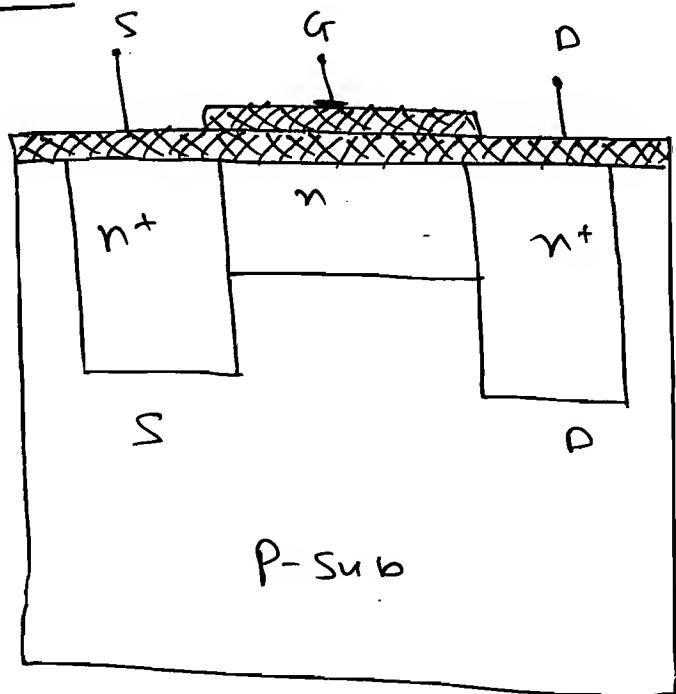
$$C_{gd} = 0 + \text{Cox} \cdot W L_{ov}$$

$$C_{gb} = \text{Cox} \cdot W L_{ov}$$



$$C_0 = \text{Cox} \times W L$$

* Linear:



$$C_{gs} = \frac{1}{2} \text{Cox} \cdot W L + \text{Cox} \cdot W L_{ov}$$

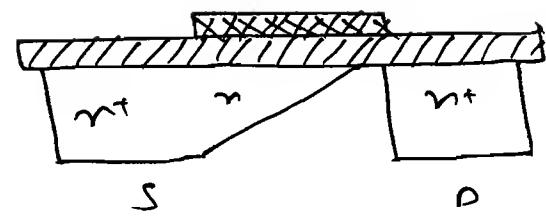
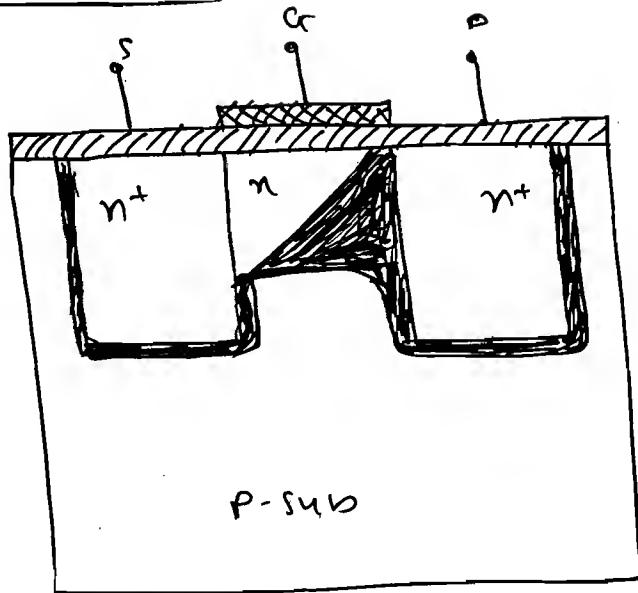
$$C_{gd} = \frac{1}{2} \text{Cox} \cdot W L + \text{Cox} \cdot W L_{ov}$$

$$L_{eff} = L - 2 \Delta L_{ov}$$

$$C_{gb} = 0 \quad \text{Here, } L \text{ is by default eff. length}$$

* Saturation:

61)



$$\Rightarrow C_{gs} = \frac{2}{3} C_{ox} W L + C_{ox} \cdot W L_{ov.}$$

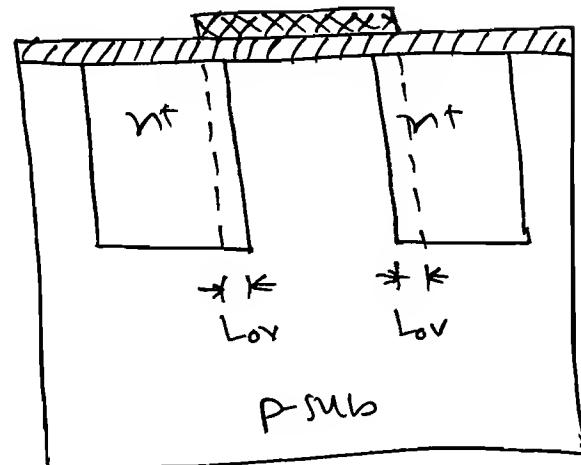
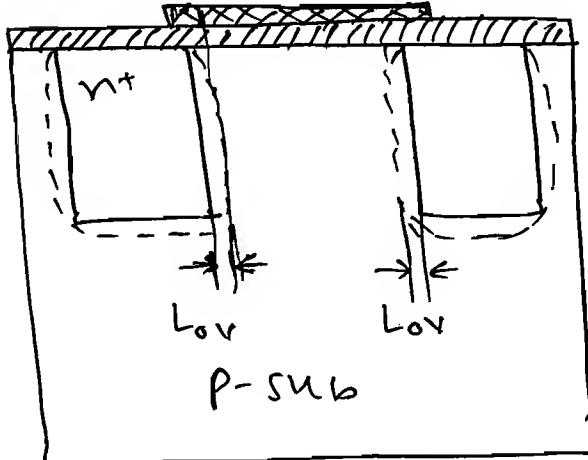
$$C_{gd} = C_{ox} \cdot W L_{ov.}$$

$$C_{gb} = 0.$$

\Rightarrow

C_{gp}	Cut off	Linear	Saturation
C_{gs}	0	$\frac{1}{2} C_0$	$\frac{2}{3} C_0$
C_{gd}	0	$\frac{1}{2} C_0$	0
C_{gb}	C_0	0	0
C_g	C_0	C_0	$\frac{2}{3} C_0$

* $L_{ov.}$: overlap Length:



$$C_{ov} = C_{ox} W L_{ov}$$

2. Junction

Capacitors:



\Rightarrow it is also called
(or) space charge

as Depletion Capacitance
Capacitance.

①

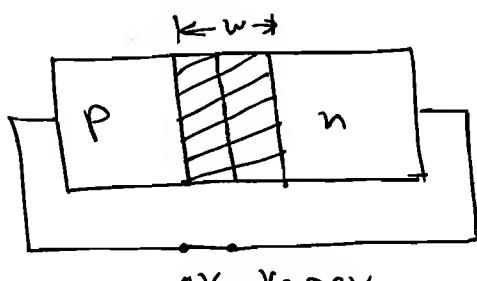


$$w$$



$$C_T = \frac{\epsilon A}{w}$$

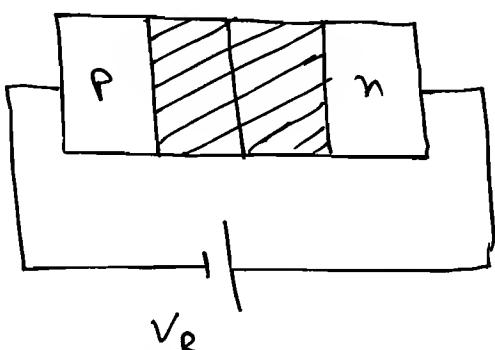
②



$$0V \quad V_R = 0V$$

$$C_{T0} = \frac{\epsilon A}{w}$$

③

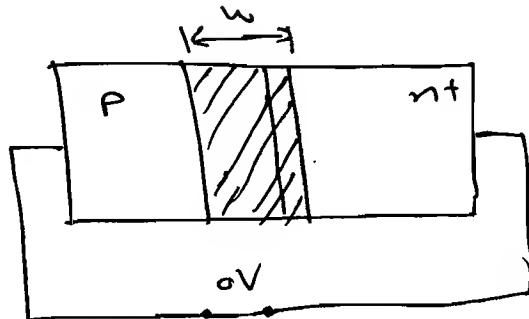


$$V_R$$

$$C_T = \frac{C_{T0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/3}}$$

$$C_{j0} = \frac{C_{j0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/3}}$$

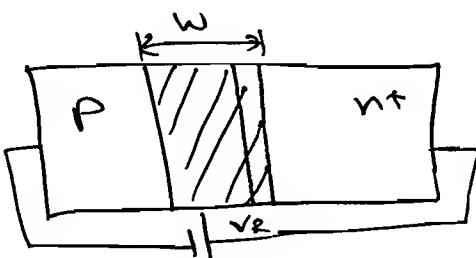
①



$$0V$$

$$C_{T0} = \frac{\epsilon A}{w} ; C_{j0} = \frac{\epsilon A}{w}$$

②



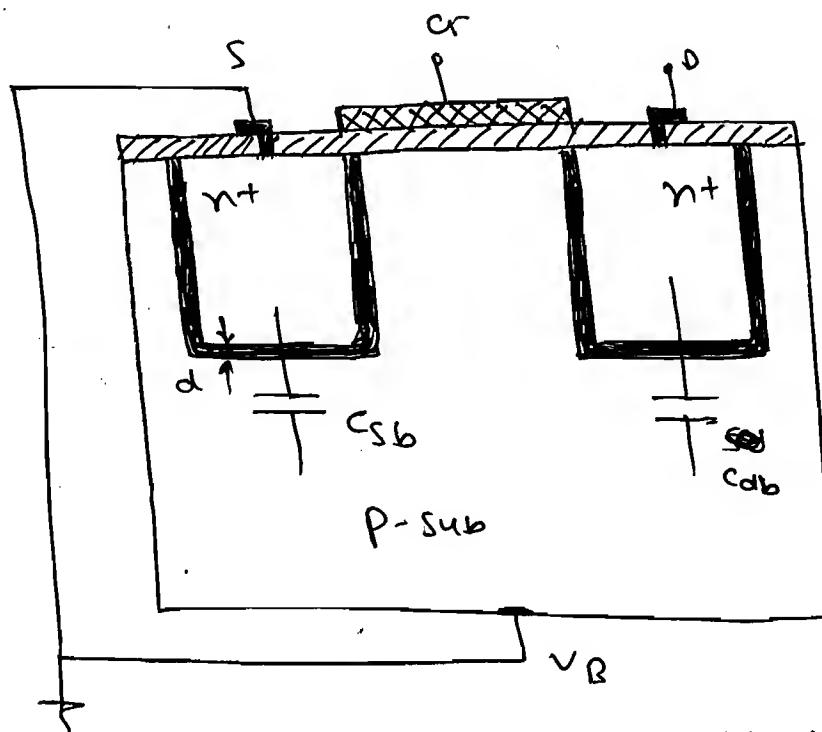
$$V_R$$

$$C_{j0} = \frac{C_{T0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/2}}$$

$$C_j = \frac{C_{j0}}{\left[1 + \frac{V_R}{V_0}\right]^{1/2}}$$

(i) Source to Body junction Capacitance:-

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$\Rightarrow V_{SB}$: Source to body Voltage.

$$C_{Sb0} = \frac{\epsilon_{Si} A}{d}$$

C_{Sb0} : Source to Body junction when

$$V_{SB} = 0V$$

A : Common area b/w source and Body.

d : depletion layer thickness b/w source and Body.

ϵ_{Si} : permittivity of Si

$$\epsilon_{Si} = \epsilon_{Si} \cdot \epsilon_0, \quad \epsilon_{Si} = 11.7 \approx 12.$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m.}$$

$$\Rightarrow C_{Sb} = \frac{C_{Sb0}}{\left[1 + \frac{V_R}{V_0}\right]^{k_2}}$$

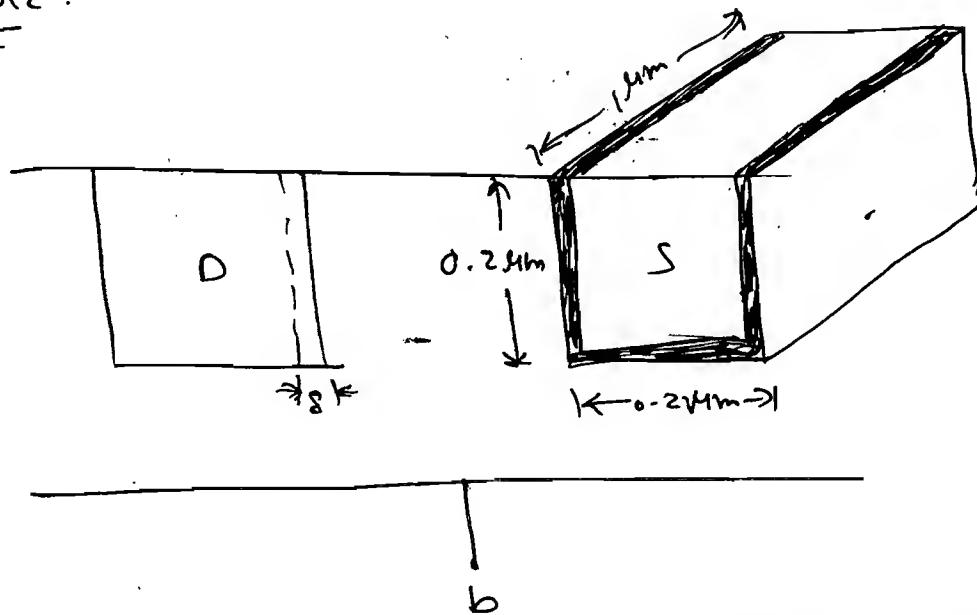
$$\therefore C_{Sb} = \frac{C_{Sb0}}{\sqrt{1 + \frac{V_R}{V_0}}}.$$

C_{sb} : Source to body Capacitance at a
 given V_{SB} .
 V_0 : Built in potential (or) contact potential.

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Q - 8



\Rightarrow In 3-dimension there are three sides at which p-n junction is created. (i) bottom (ii) Left (iii) Right. So, we should consider total area betⁿ body and source for C_{sb} calculation.

\therefore and here no biasing is provided

$$\therefore C_{sb} = C_{sbo} = \frac{E_s \cdot A}{d}$$

$$\begin{aligned}
 \therefore A &= (0.2 \mu m \times 0.2 \mu m) + (0.2 \times 1 \mu m) + (0.2 \mu m \times 1 \mu m) \\
 &= 3 \times 0.2 \times 10^{-6} \times 1 \times 10^{-6}
 \end{aligned}$$

$$\therefore A = 0.6 \times 10^{-12} \text{ m}^2.$$

$$\therefore C_{sb} = \frac{11.7 \times 8.9 \times 10^{-12} \times 0.6 \times 10^{-12}}{10 \times 10^{-9}}$$

$$\therefore C_{sb} = 6.24 \times 10^{-15}$$

$$\therefore C_{SB} = 6.24 \text{ fF} \approx 7 \text{ fF}$$

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if we consider boost and buck area
then $A = (3 \times 0.2 \times 10^{-12}) + (2 \times 0.2 \times 0.2 \times 10^{-12})$
 $A = 0.68 \times 10^{-12} \text{ m}^2$

2

$$C_{SB} = 7.024 \text{ fF}$$

(Q-9)

Soln:

$$C_{GSov} = \frac{\epsilon_{SiO_2} W L_{ov}}{d}$$

$$C_{GSov} = \frac{3.9 \times 8.9 \times 10^{-12} \times 10^{-6} \times 20 \times 10^{-9}}{10 \times 10^{-9}}$$

$$\therefore C_{GSov} = 0.7 \text{ fF.}$$

2. Drain to Body in Capacitor:

$\Rightarrow V_{DB} = \text{Drain to Body voltage.}$

$$C_{DB0} = \frac{\epsilon_{Si} A}{d}$$

C_{DB0} = drain to body capacitance when

$$V_{SB} = 0.$$

d : depletion layer thickness betⁿ D & S.

A : common area betⁿ D & S.

ϵ_{Si} : permittivity of Si

$$\epsilon_{Si} = \epsilon_{Si} \cdot \epsilon_0, \quad \epsilon_{Si} = 11.7 \approx 12.$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m.}$$

\Rightarrow

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{db}}{V_0}}}.$$

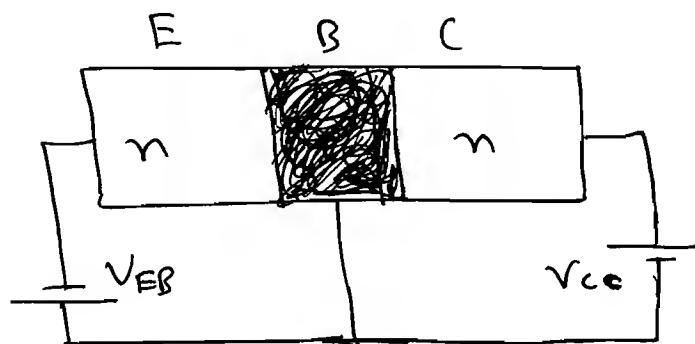
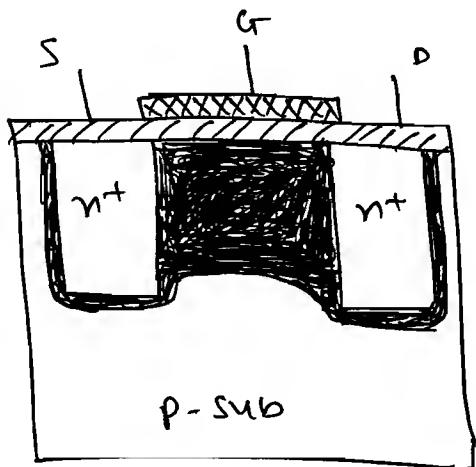
C_{db} : Drain to body Capacitor with a
given V_{GB} .

V_0 : Built in potential at constant
potential.

* Short channel effect :-

1. Punch through:

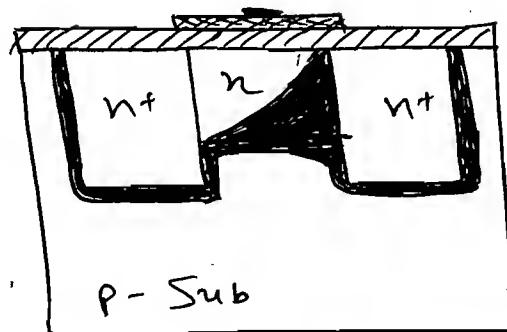
\Rightarrow



\Rightarrow For short channel MOSFET in the saturation region as drain to source voltage increases. The width of the drain depletion region increases. At a particular value of V_{DS} , drain depletion region penetrates through channel to the source. It is called punch through (02).

2. Avalanche Break Down:

⇒



⇒ As drain to source voltage increases, the width of the drain depletion region increases. At a particular value of V_{DS} , this depletion region gets breakdown due to avalanche effect. Therefore, it is called avalanche effect.

⇒ Due to punch through effect (or) Avalanche Breakdown, the MOSFET never gets damage.

3. Gate-oxide Break-Down:

⇒ As gate to source voltage increases at a particular value of V_{GS} the oxide layer betⁿ gate and source gets damage (or) Breakdown it is called gate-oxide Breakdown.

⇒ Gate oxide B-D is a permanent damage to the MOSFET.

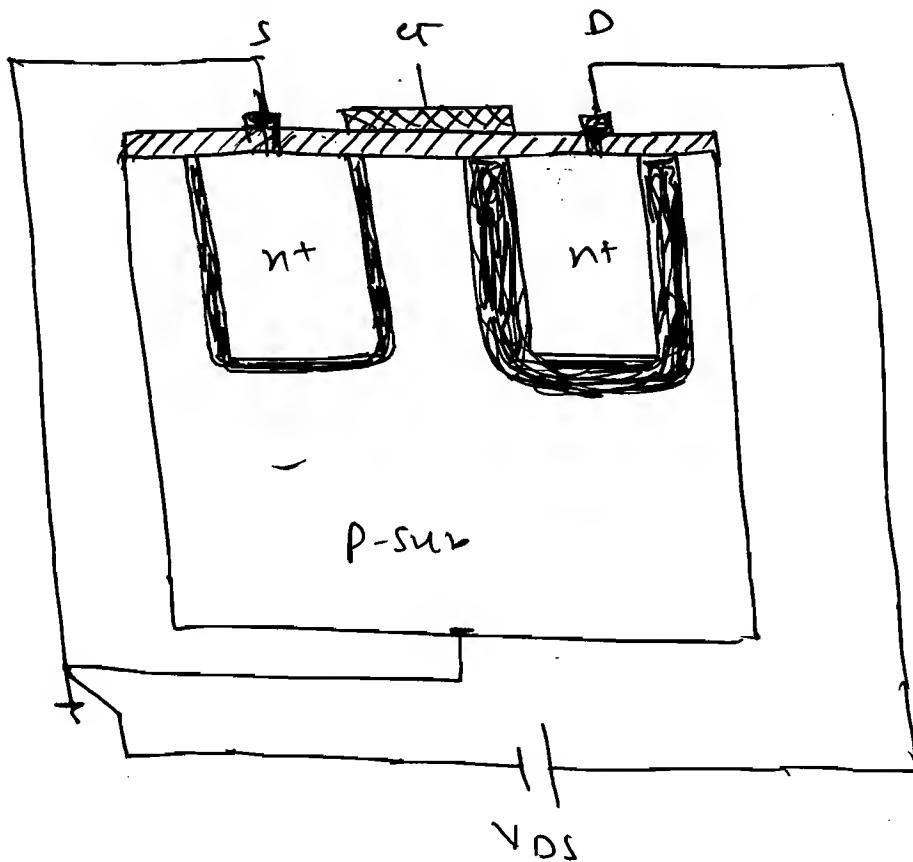
4. Drain

Induced

Barrier

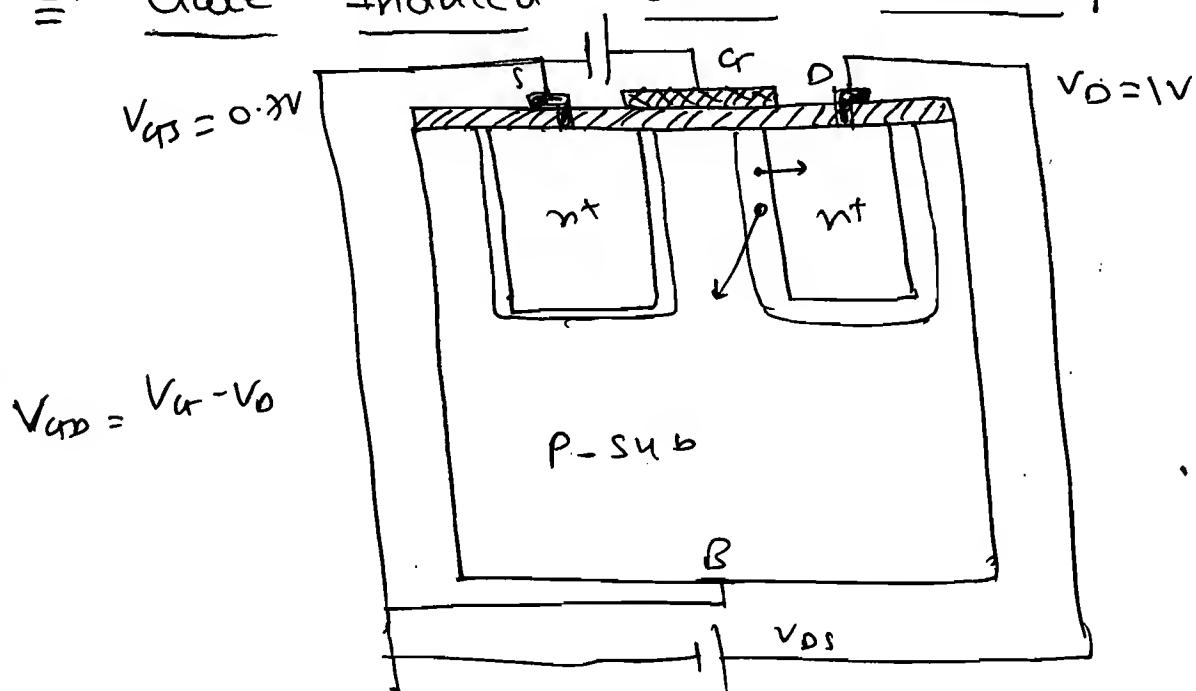
Lowering (DIDL):

⇒

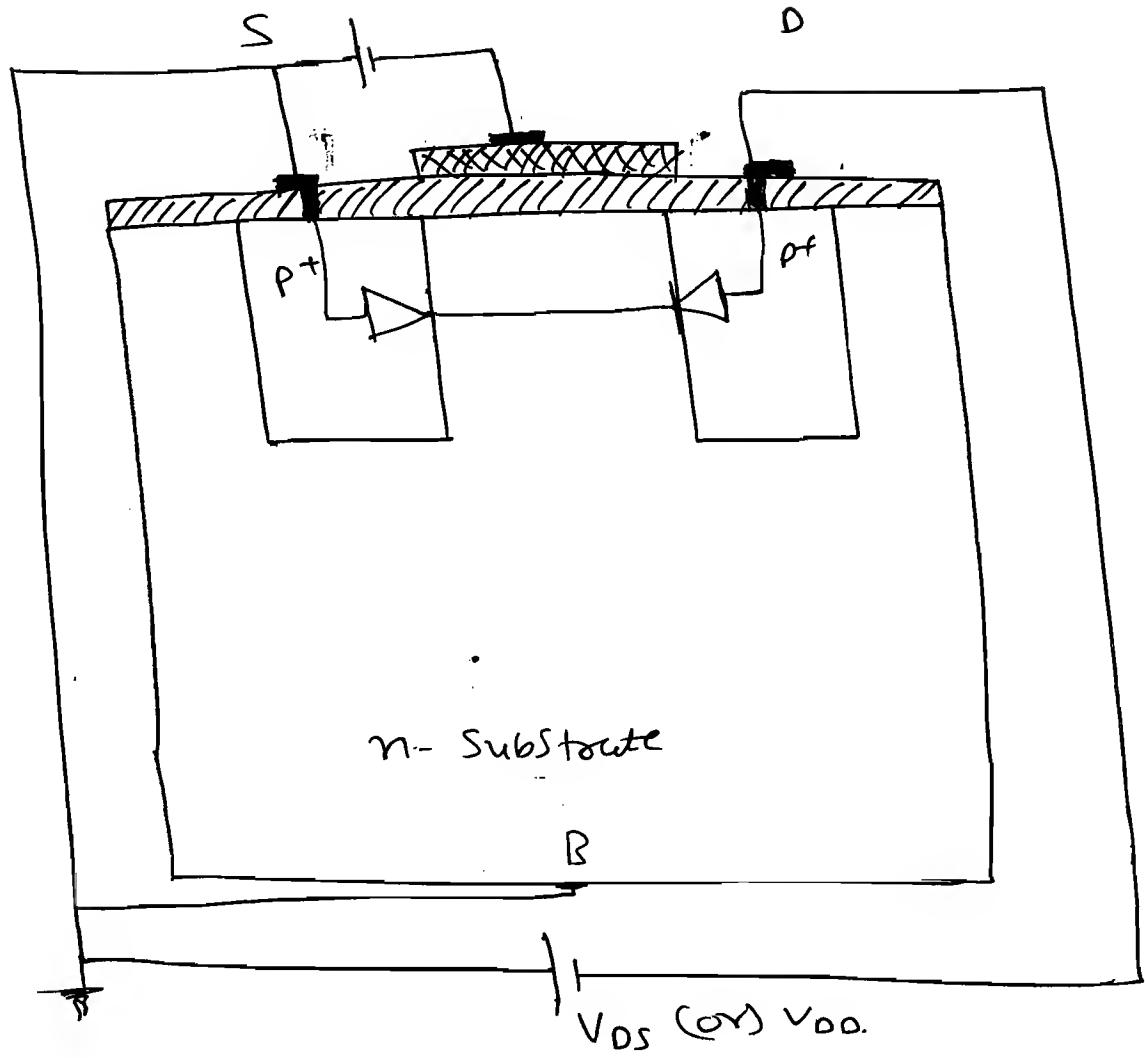


⇒ As drain to source voltage increases the width of the drain depletion region increases. Therefore, threshold voltage decreases. i.e. it forms a channel for lower value of V_{th} .

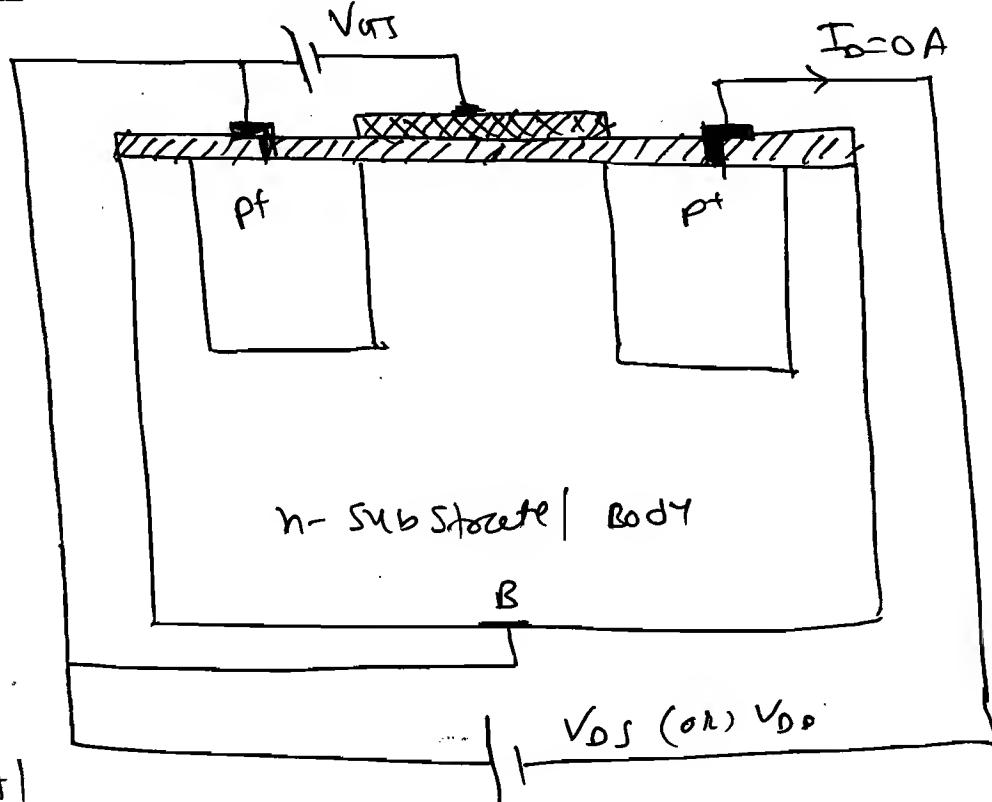
5. Gate Induced drain Leakage ; (GIDL).



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 ~ P- channel ~ Enhancement ~ MosFET:



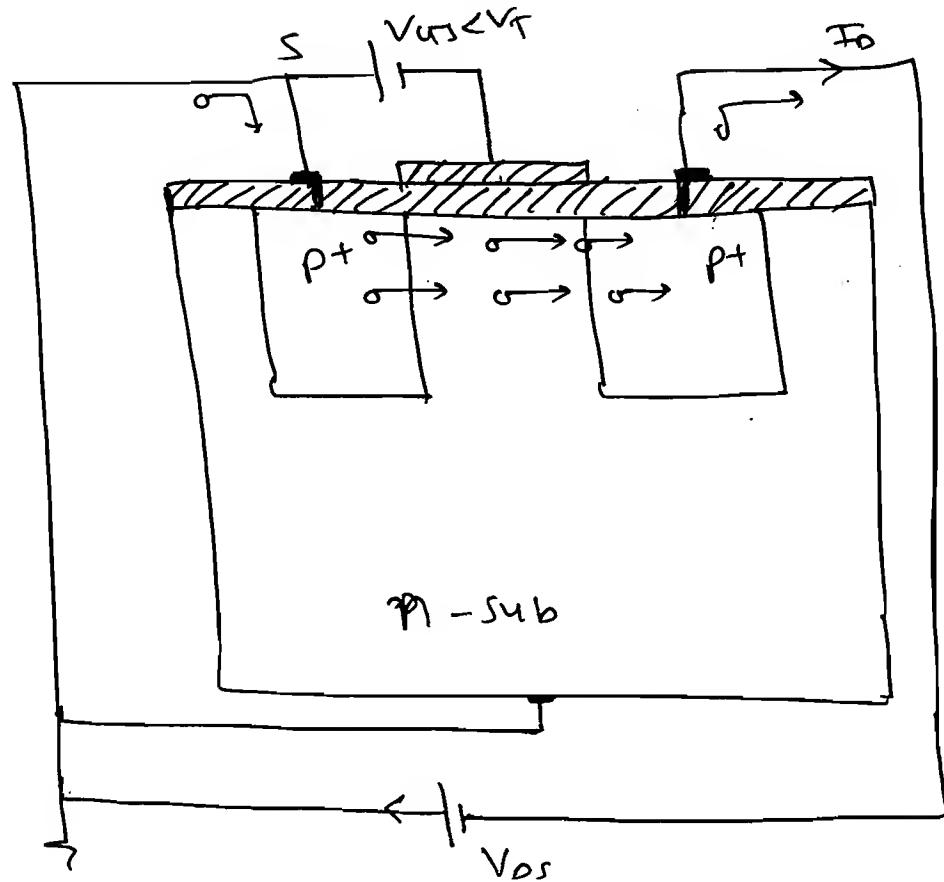
① $V_{GS} > V_T$: Cut-off:



$$|V_{GS}| < |V_T|$$

②

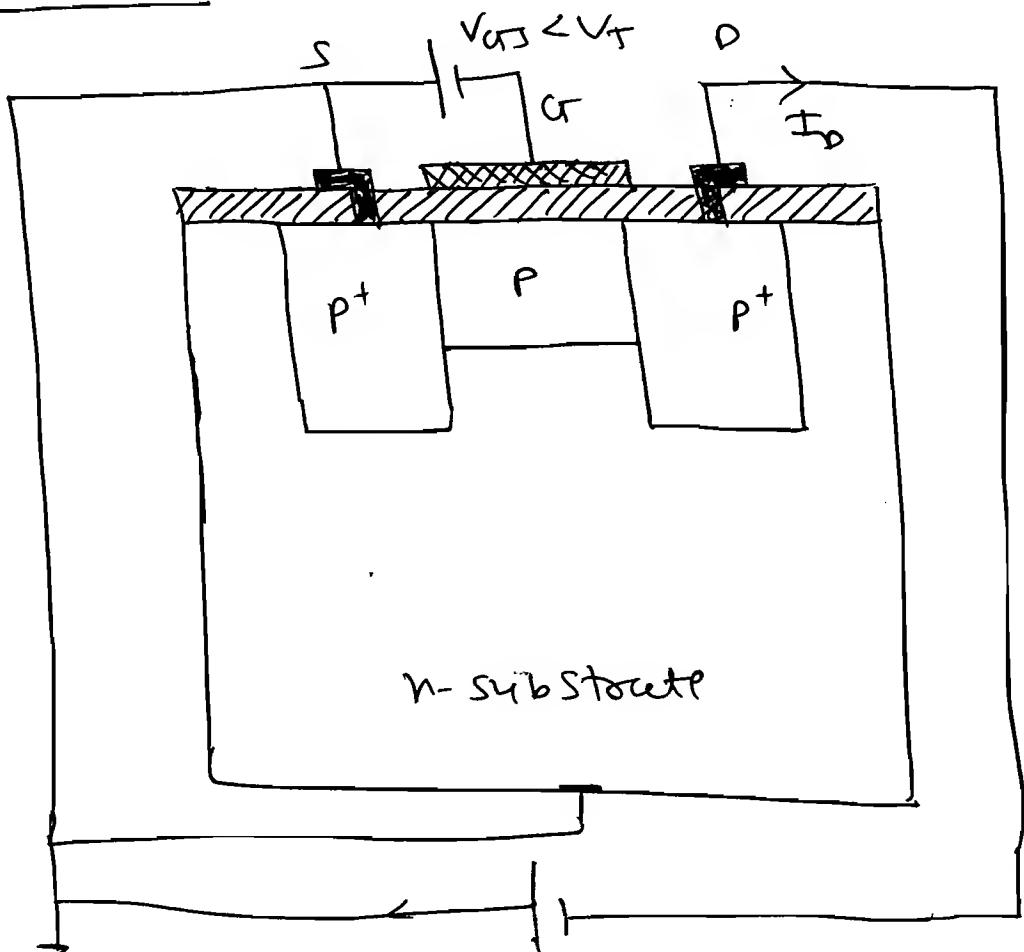
$$\underline{V_{GS} < V_T} \quad \& \quad \underline{V_{DS} > V_{GS} - V_T} : \underline{\text{Linear.}}$$



$$|V_{GS}| > |V_T| \quad \& \quad |V_{DS}| < |V_{GS} - V_T|.$$

③

$$\underline{V_{GS} < V_T} \quad \& \quad \underline{V_{DS} < V_{GS} - V_T} : \underline{\text{Saturation.}}$$

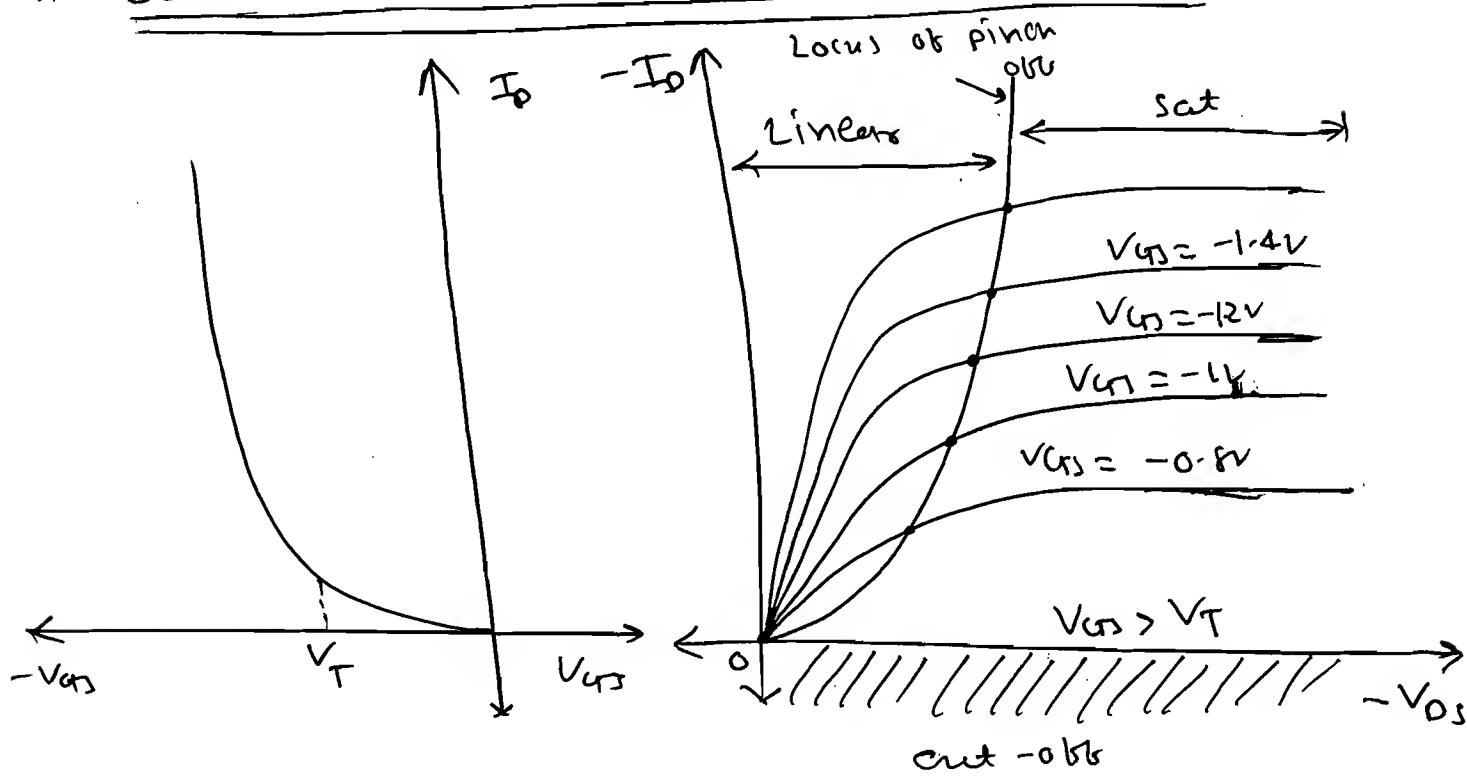


$$\Rightarrow |V_{GS}| < |V_T| \quad \& \quad |V_{DS}| > |V_{GS} - V_T|.$$

66)

$$V_{DS} = -ve, \quad V_{GS} = -ve, \quad V_T = -ve.$$

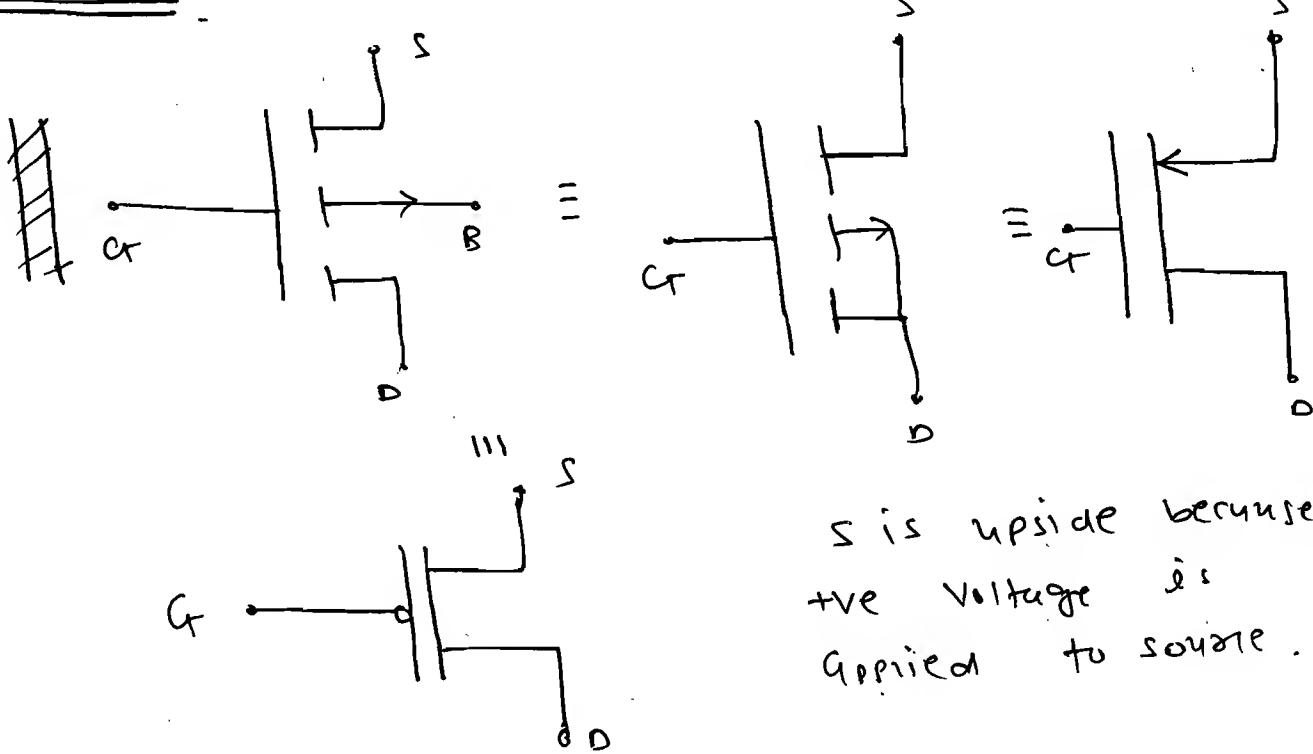
* Drain and Transfer Characteristics



Transfer Characteristics

Drain Characteristics

* Symbol:



S is upside because
+ve voltage is
applied to source.

* Condition for pinch-off:

$$\Rightarrow V_{DS} = V_{GS} - V_p$$

↑ ↑ ↑
-ve -ve -ve

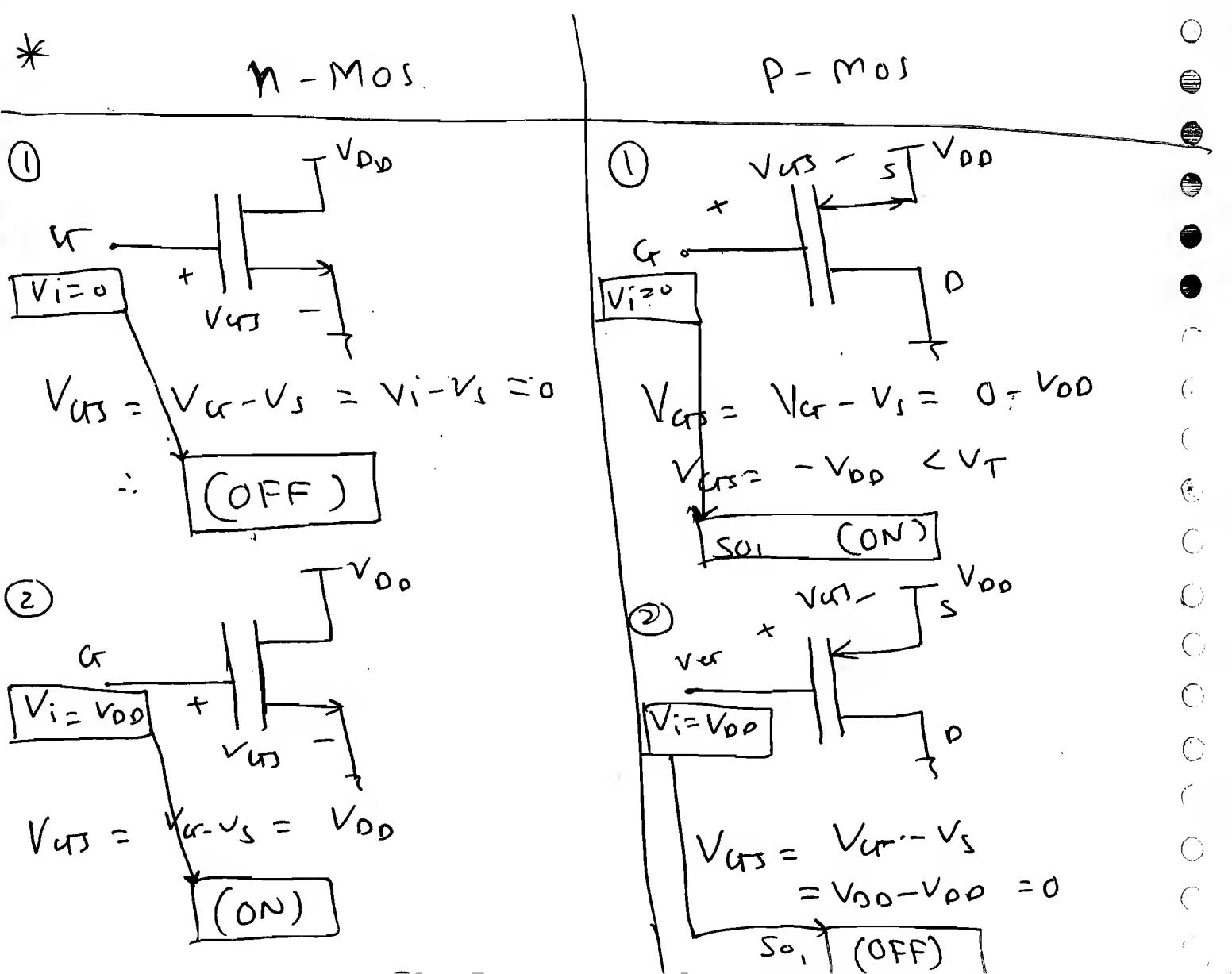
$$\Rightarrow V_{DS} > V_{GS} - V_p : \text{Linear}$$

$$V_{DS} < V_{GS} - V_p : \text{Sat.}$$

*

n-Mos		P-Mos
$V_{GS} = 0$	OFF	OFF
$V_{GS} = +ve$ i.e. $(V_{GS} > V_T)$:	ON	OFF
$V_{GS} = -ve$ i.e. $(V_{GS} < V_T)$:	OFF	ON

*



* Imp Points to be remember:

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⇒ P-Channel MOSFET operates with -ve gate voltages i.e. -ve V_{GS} values.

⇒ Gate-to-source voltage (i.e. V_{GS}) and threshold voltage (V_T) are -ve for P-channel enhancement MOSFET.

⇒ P-Channel EMOSFET operates in enhancement mode for -ve V_{GS} values.

⇒ In discrete P-EMOSFET, substrate (or) Body (or) Bulk is connected to source terminal (or) V_{DD} . whereas in ICs it should be connected to most +ve values.

⇒ P-EMOSFET will be on for -ve V_{GS} values (i.e. $V_{GS} < V_T$) and it will be OFF for 0 or +ve V_{GS} values i.e. ($V_{GS} > V_T$)

⇒ Condition for pinch-off (or) saturation is $V_{DS} = V_{GS} - V_T$. and here, all are -ve.

⇒ For $V_{GS} > V_T$ (or) $|V_{GS}| < |V_T|$. P-MOSFET operates in cut-off region and its drain current $I_D = 0$.

⇒ For $V_{GS} < V_T$ and $V_{DS} > V_{GS} - V_T$ (or) $|V_{GS}| > |V_T|$ and $|V_{DS}| < |V_{GS} - V_T|$

it operates in linear region and its drain current

$$I_D = \mu_p \cdot C_{ox} \cdot \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

↑-ve ↑-ve

μ_p : mobility of holes.

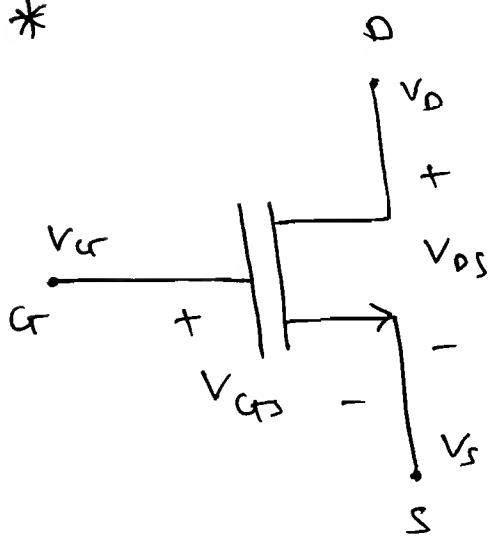
\Rightarrow For $V_{GS} < V_T$ & $V_{DS} \leq V_{GS} - V_T$ (or)

$|V_{GS}| > |V_T|$ & $|V_{DS}| \leq |V_{GS} - V_T|$. it operates in saturation region and its drain current,

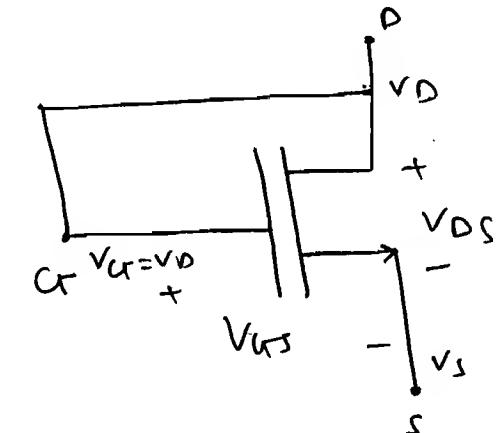
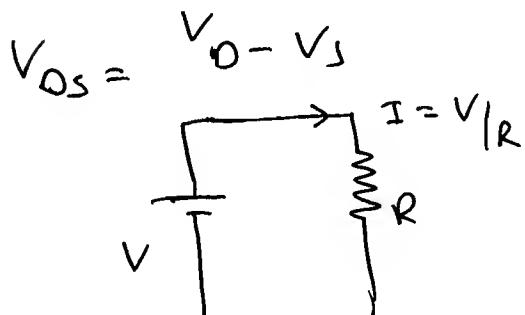
$$I_D = \frac{1}{2} \mu_p \cdot C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2$$

↑-ve ↑-ve

*

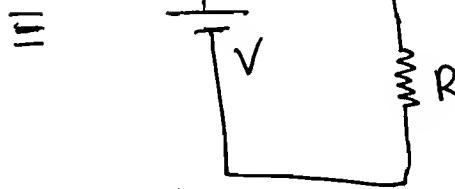
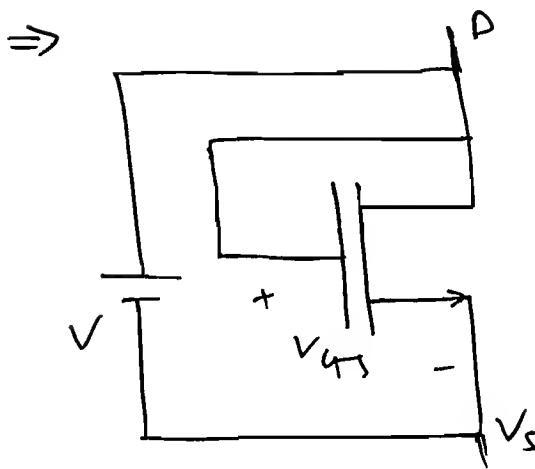


$$V_{GS} = V_G - V_S$$



$$\rightarrow \text{if } V_G = V_D \Rightarrow V_{GS} = V_{DS}$$

$$\rightarrow \text{if } V_{GS} = V_{DS} \text{ and } V_{GS} > V_T \Rightarrow \text{Sat}$$

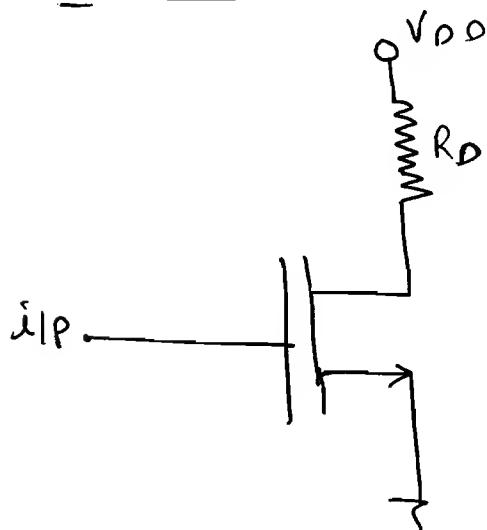


$$V_{GS} = V > V_T$$

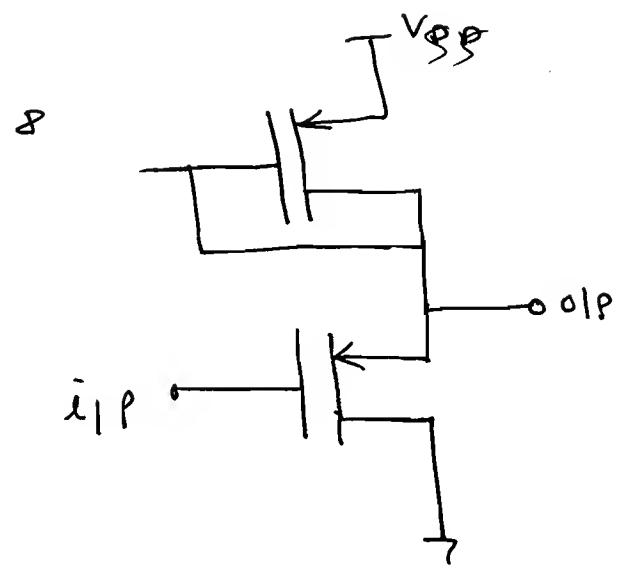
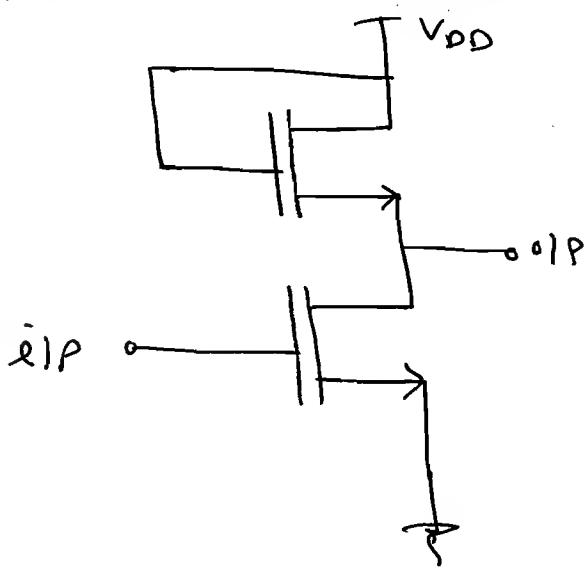
then I will flow.

★ Types of Load:

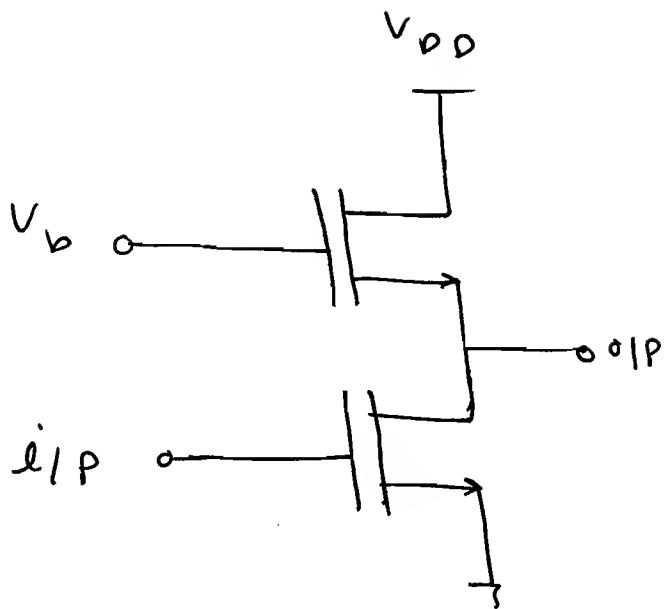
① Resistive Load:



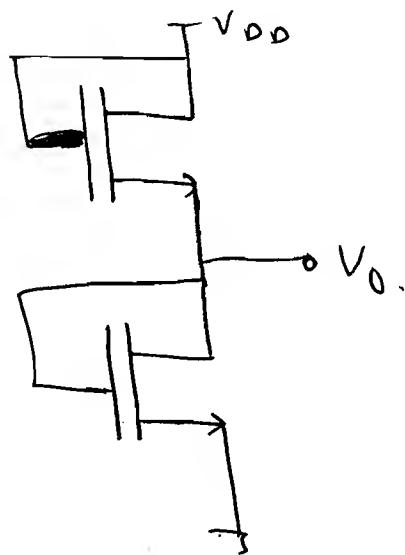
② Diode Connected Load:



③ Current-Source Load:



Q) Find V_o in the given figure.



Solⁿ: Both are n-channel and same parameters. So, both are ~~series~~ act as a sum resistor. Hence $V_o = \frac{V_{DD}}{2}$.

CMOS

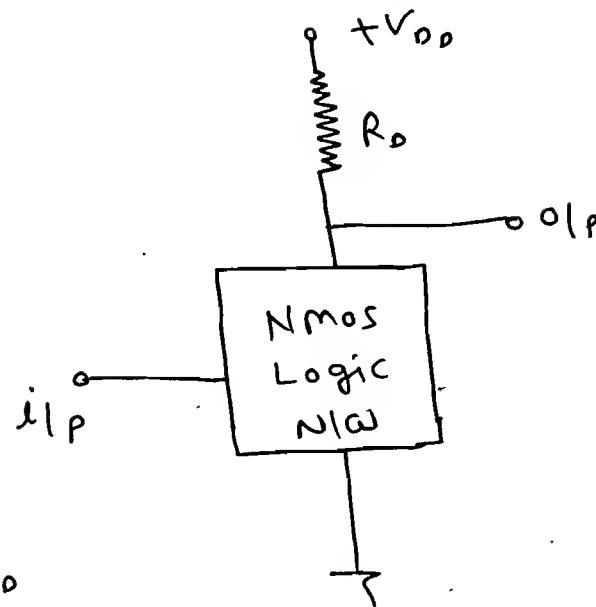
(complementary MOS):

69)

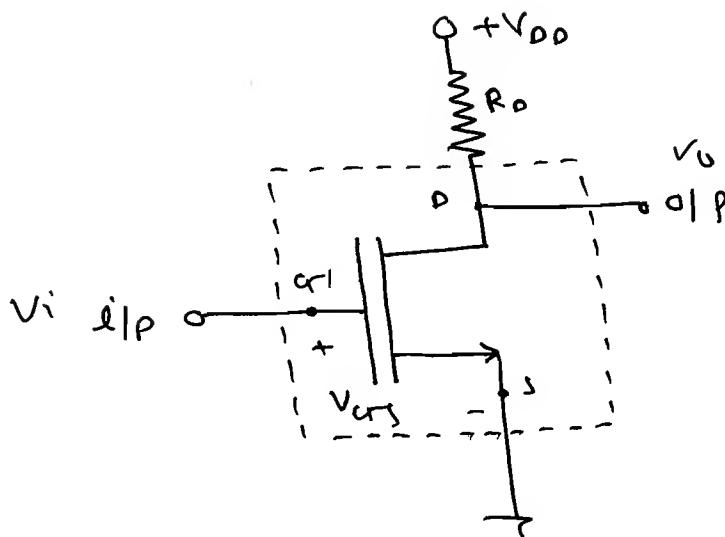
* n-MOS:

⇒ Inverter:

A	$Y = \bar{A}$
0	1
1	0



⇒

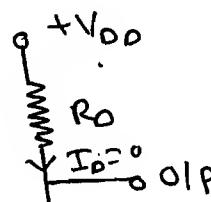


$$(i) \quad V_i = 0$$

$$V_{GS} = V_G - V_S = V_i - 0$$

$$V_{GS} = 0$$

⇒ **[OFF]**

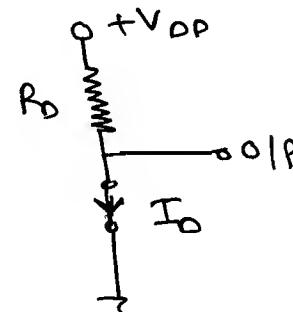


$$(ii) \quad V_i = +V_{DD}$$

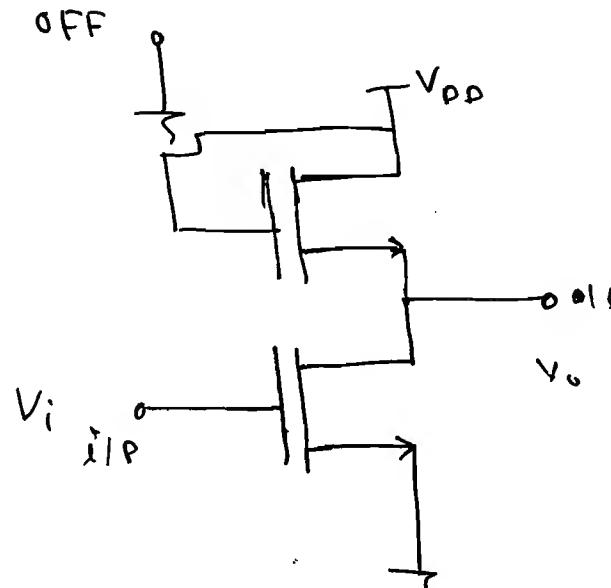
$$V_{GS} = V_G - V_S = V_i - 0$$

$$V_{GS} = V_{DD}$$

⇒ **[ON]**

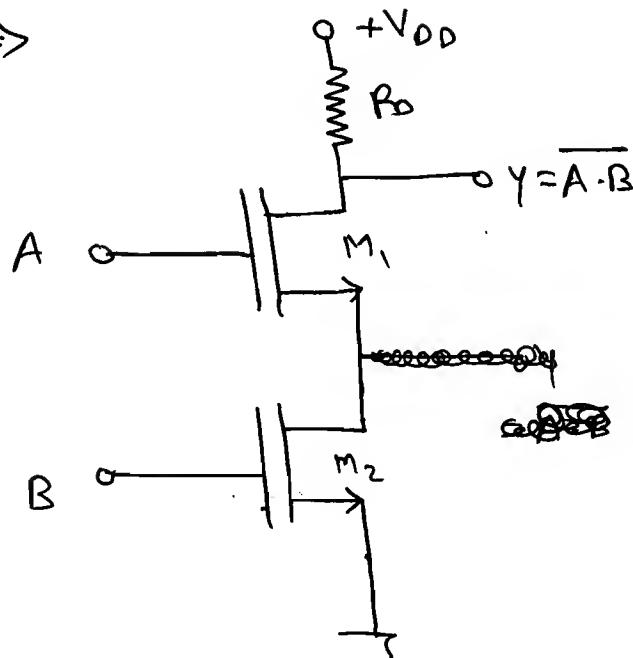


⇒



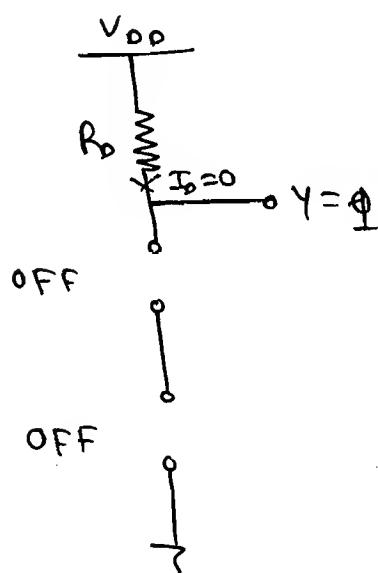
* 2- Input NAND Gate:-

⇒

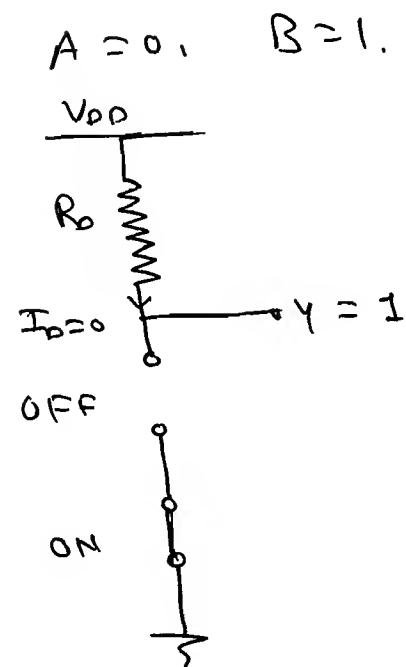


		$F = \overline{A \cdot B}$
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

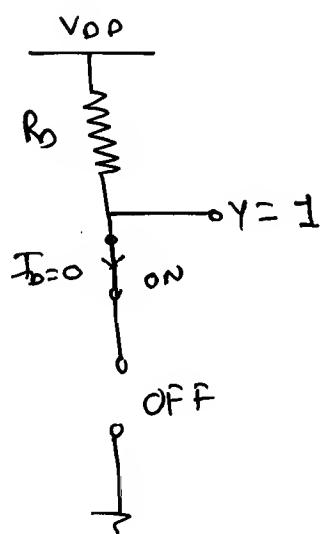
⇒ (i) V_i , $A = 0, B = 0$.



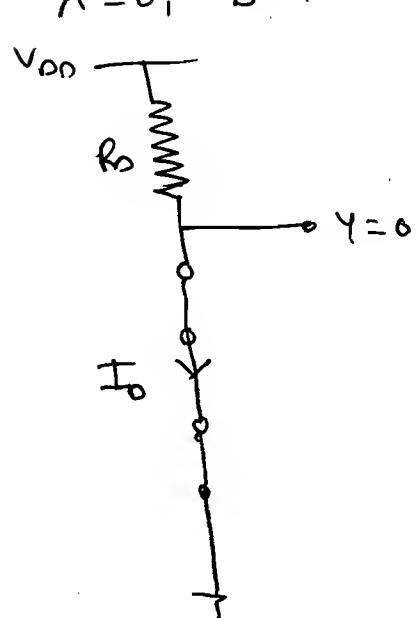
(ii) $A = 0, B = 1$.



(iii) $A = 1, B = 0$

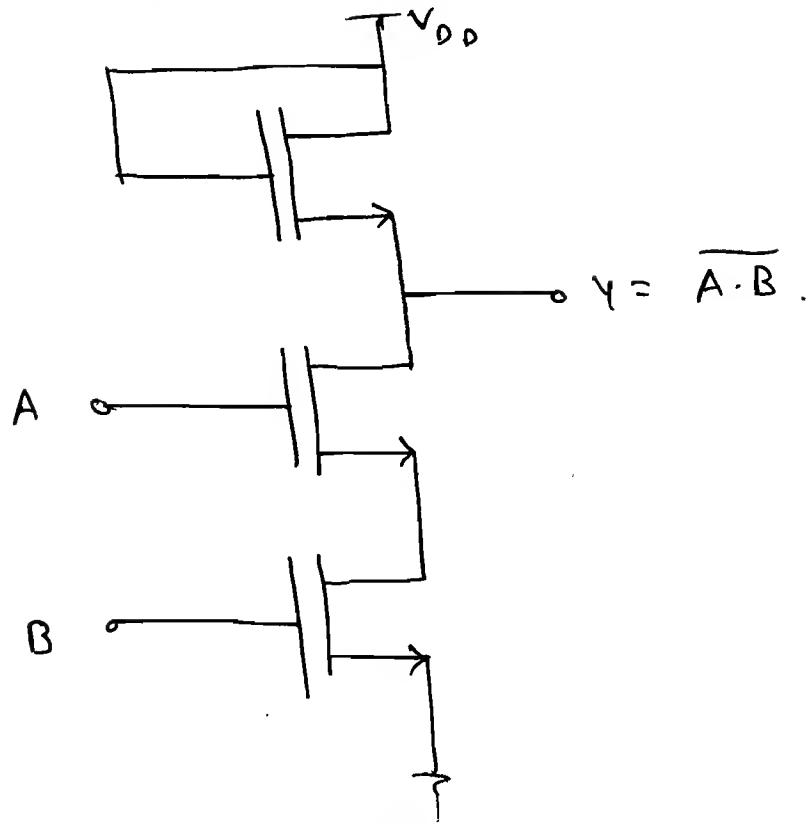


(iv) $A = 0, B = 1$



⇒ Replace R_o by one more nmos.

⇒



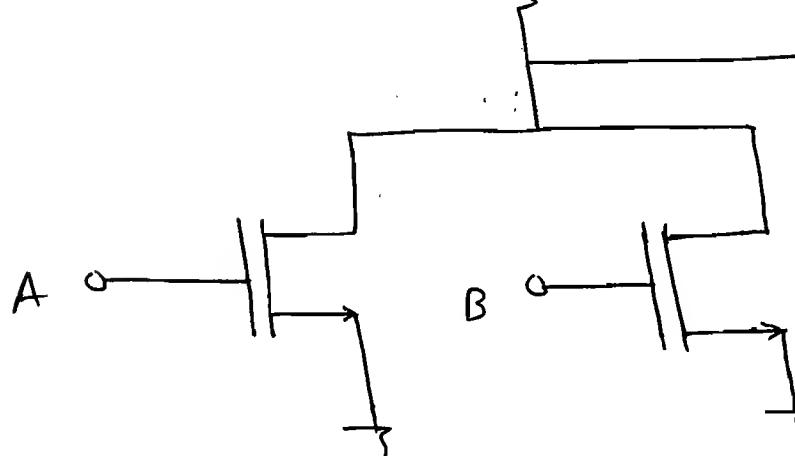
* 2-input

NOR

Gate:

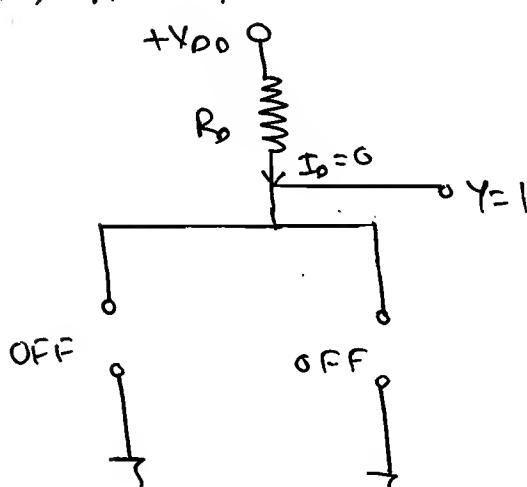
$$A + V_{DD}$$

⇒

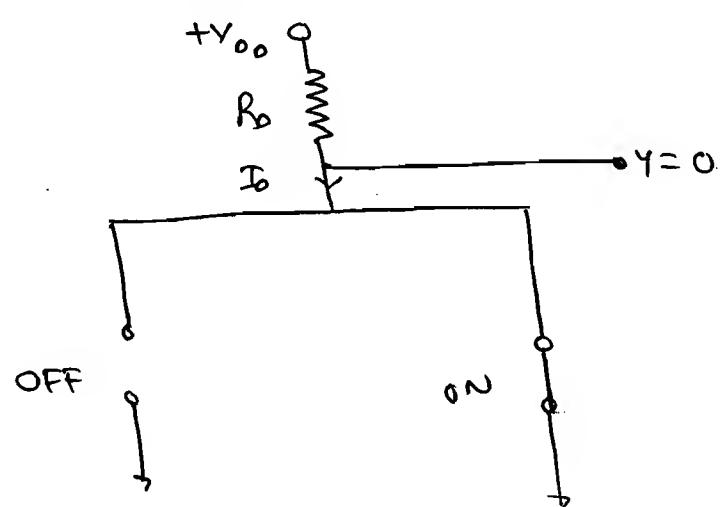


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

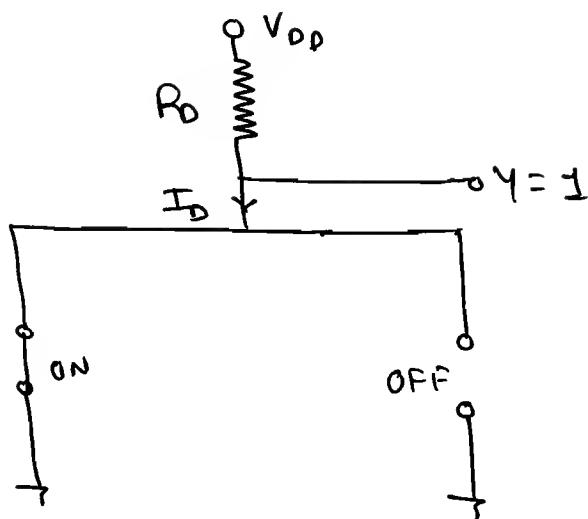
(i) $A = 0, B = 0$.



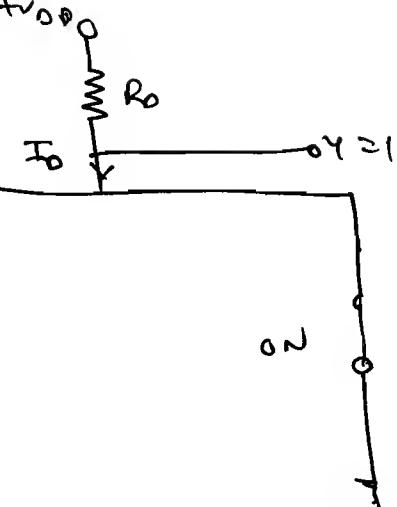
(ii) $A = 0, B = 1$.



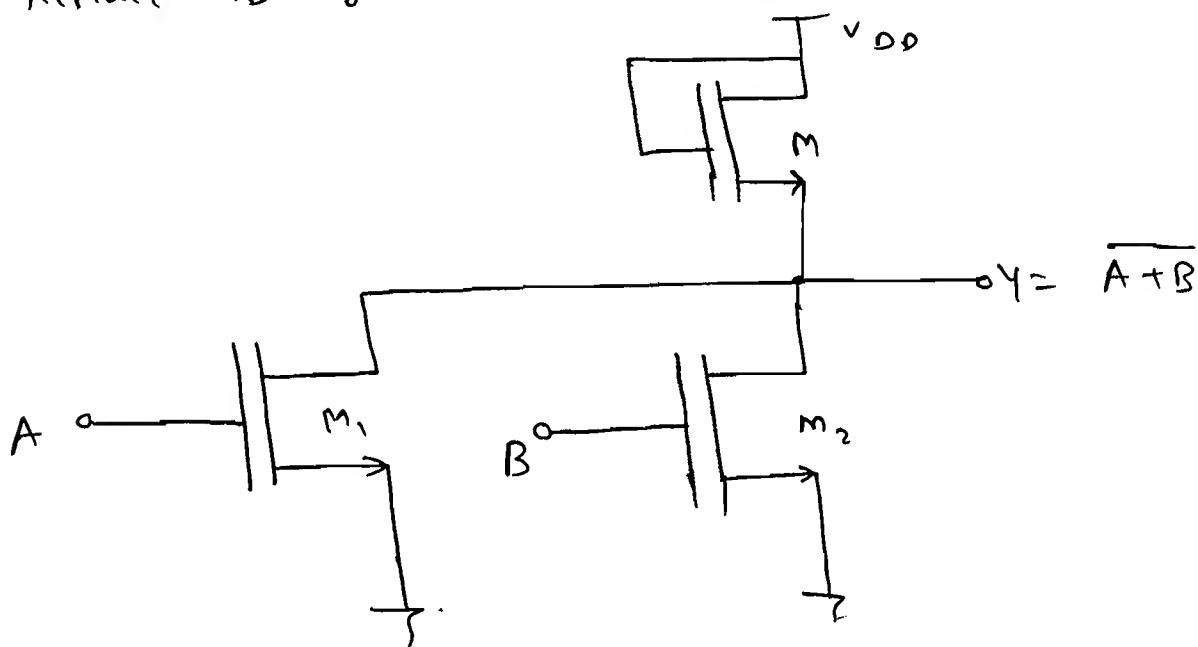
(iii) $A = 1, B = 0$



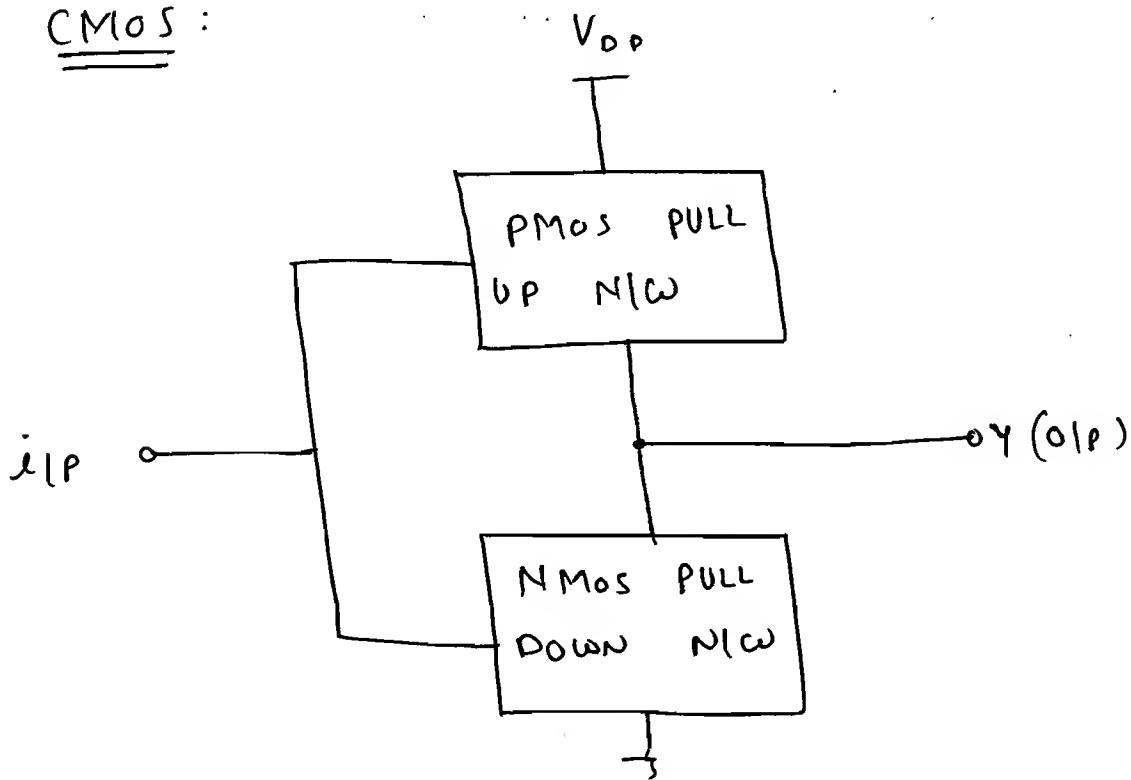
(iv) $A = 1, B = 1$



\Rightarrow Replace R_D by one more NMOS.

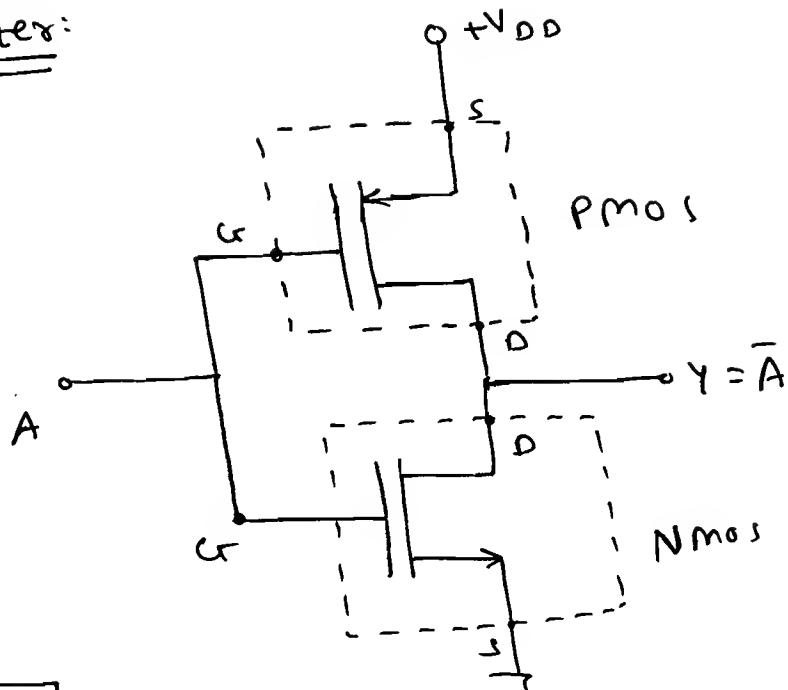


* CMOS:



* Inverter:

⇒



(i) $V_i = 0$

Nmos

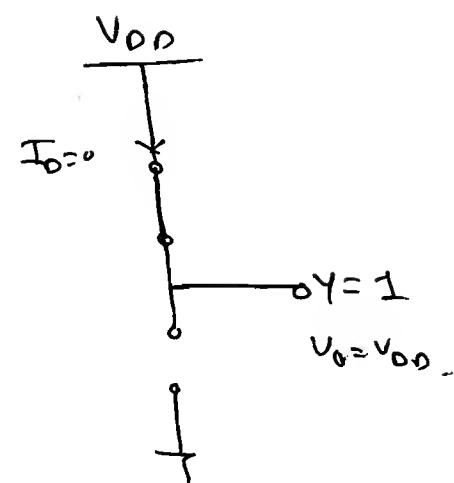
$$V_{GSS} = V_{GS} - V_S \\ = V_i - 0 \\ V_{GSS} = V_i = 0$$

OFF

PMOS

$$V_{GSS} = V_{GS} - V_S \\ = V_i - V_{DD} \\ V_{GSS} = -V_{DD}$$

ON



(ii) $V_i = +V_{DD}$

Nmos

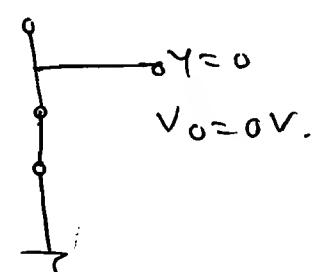
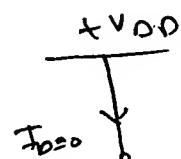
$$V_{GSS} = V_{GS} - V_S \\ = V_{DD} - 0 \\ V_{GSS} = V_{DD}$$

⇒ ON

PMOS

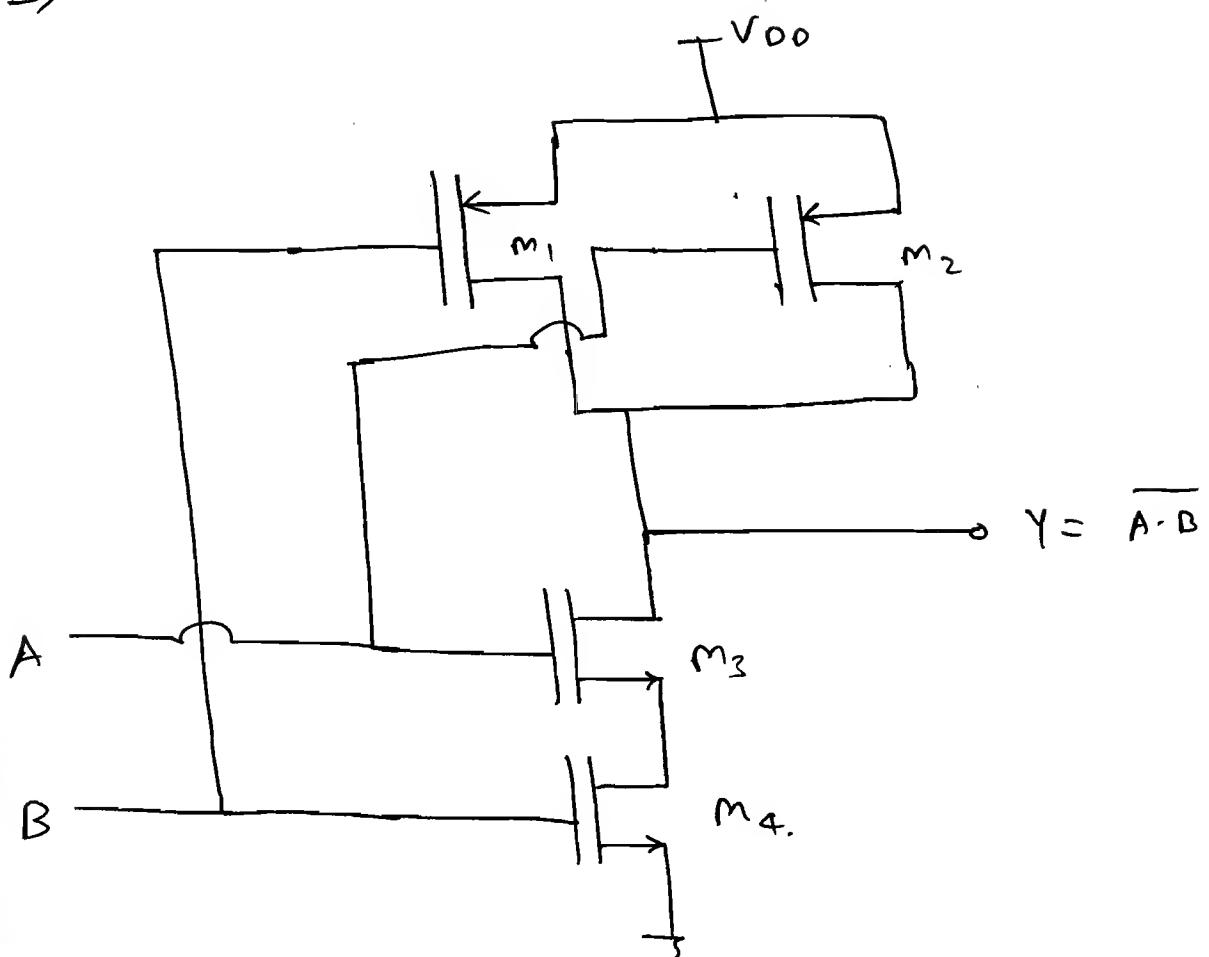
$$V_{GSS} = V_{GS} - V_S \\ = V_{DD} - V_{DD} \\ V_{GSS} = 0$$

⇒ OFF

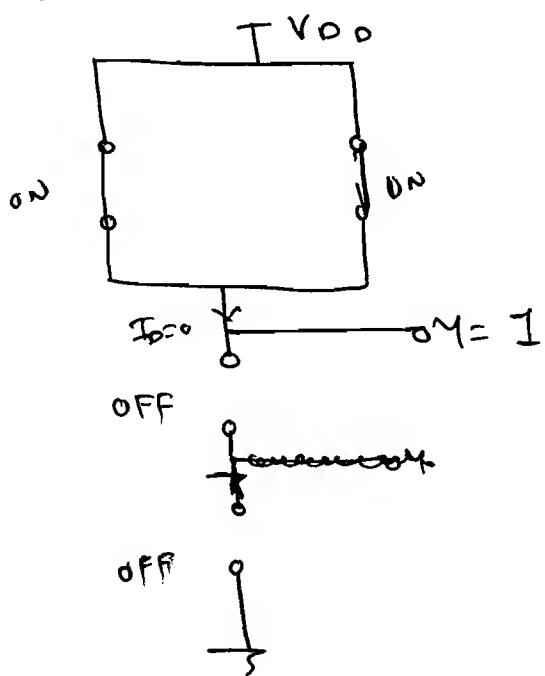


⇒ Here in both the case ideally I_D is zero. But practically some small power is dissipated in T_x . But is very small compare to other technology.

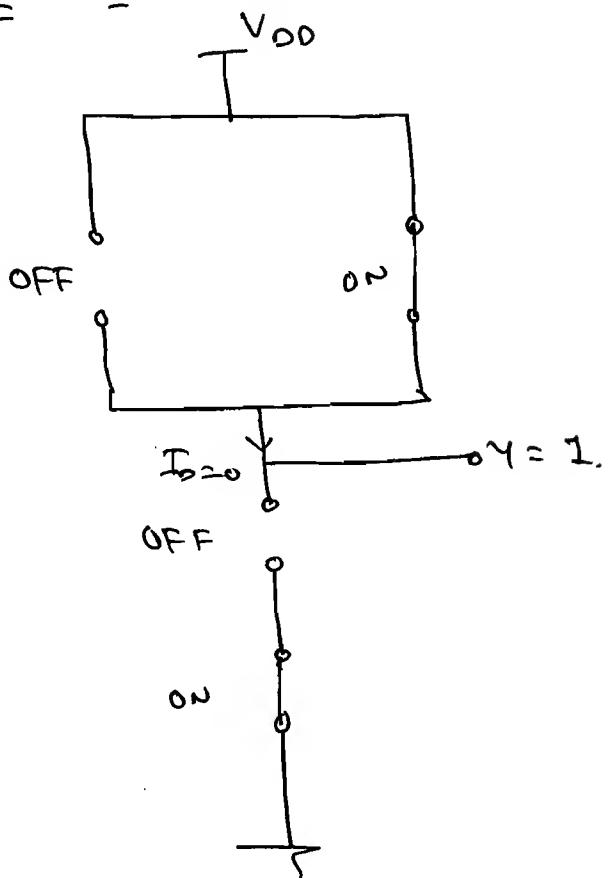
* 2 elp NAND gute:
 \Rightarrow



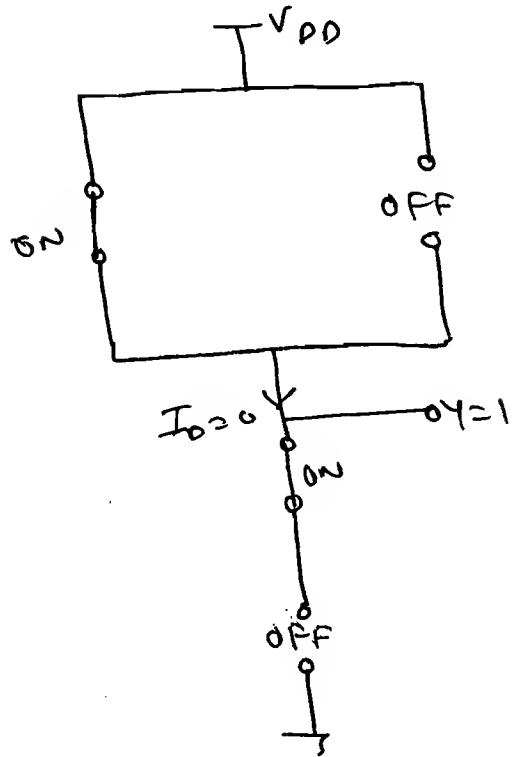
Case - (i) $A = 0, B = 0.$



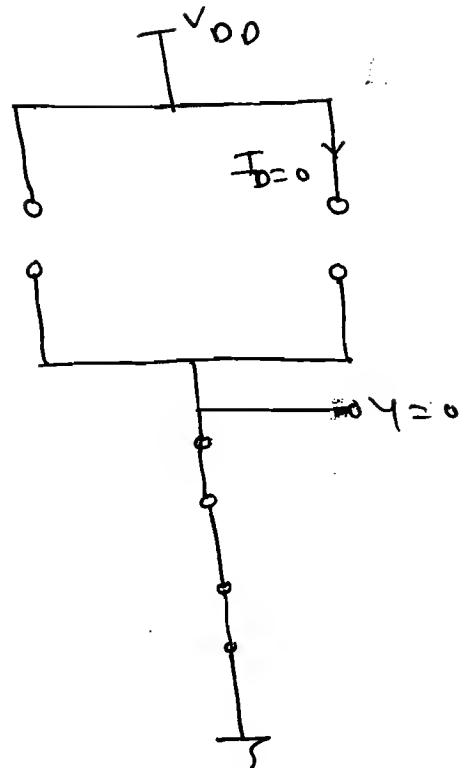
Case - (ii) $A = 0, B = 1$



(iii) $A=1, B=0$

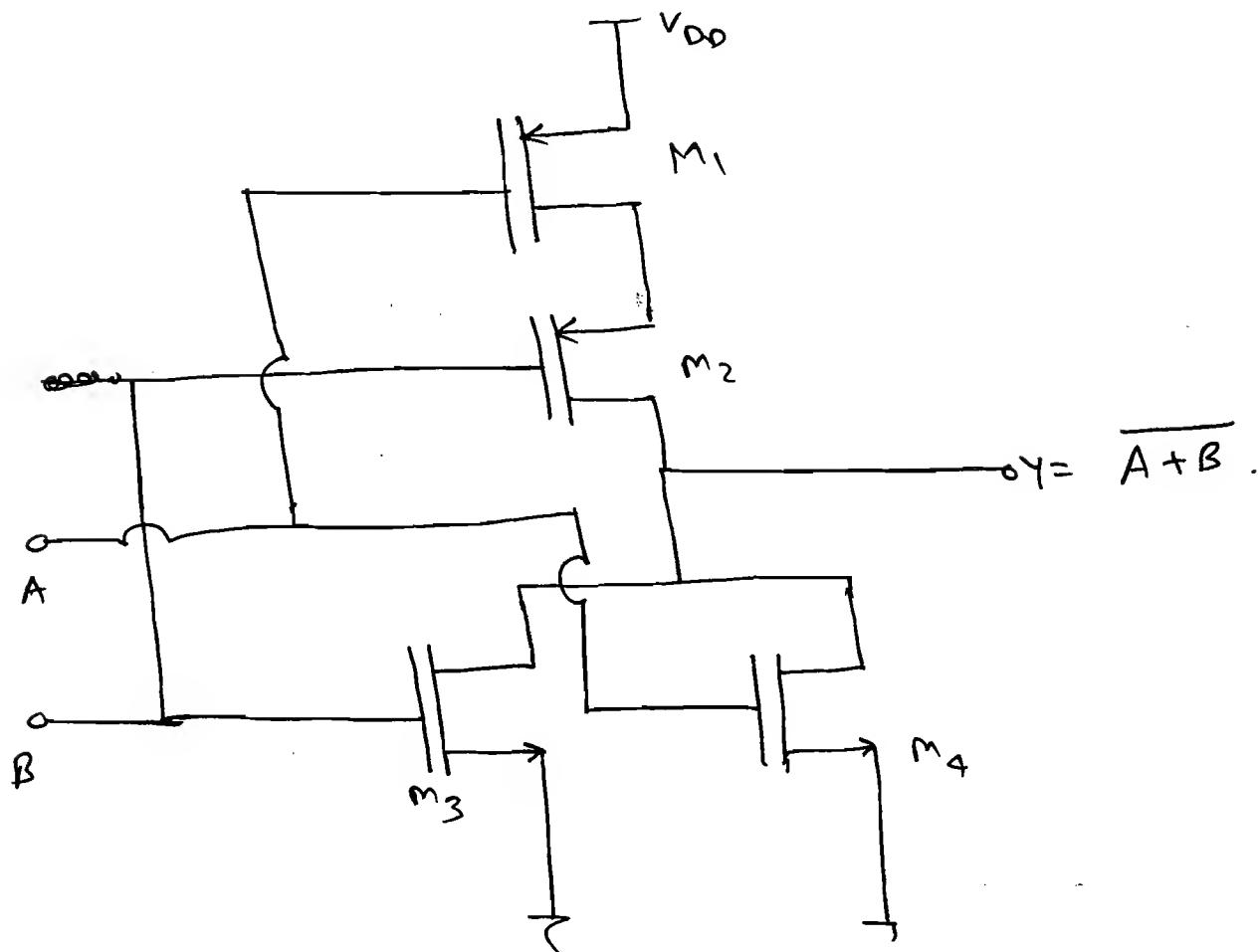


(iv) $A=1, B=1$

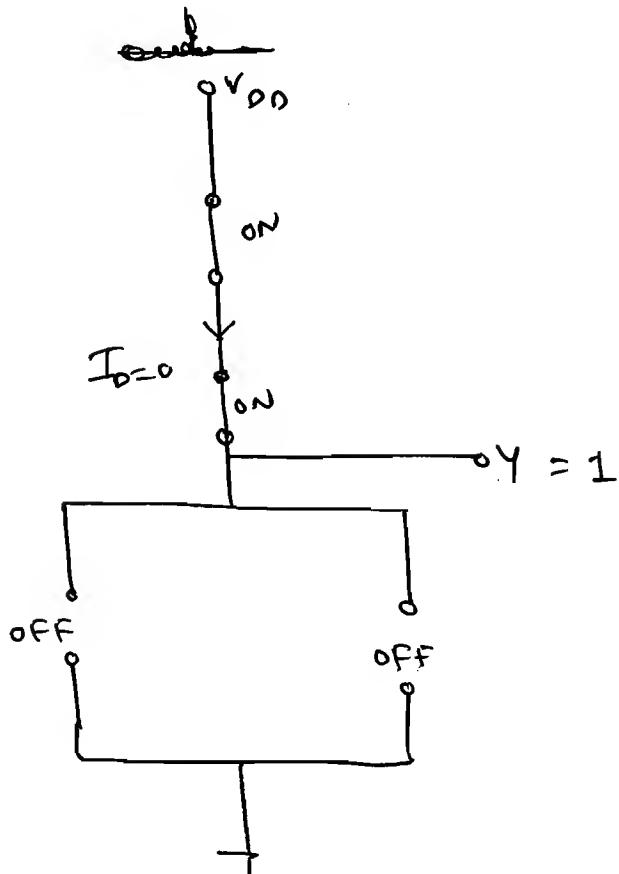


72)

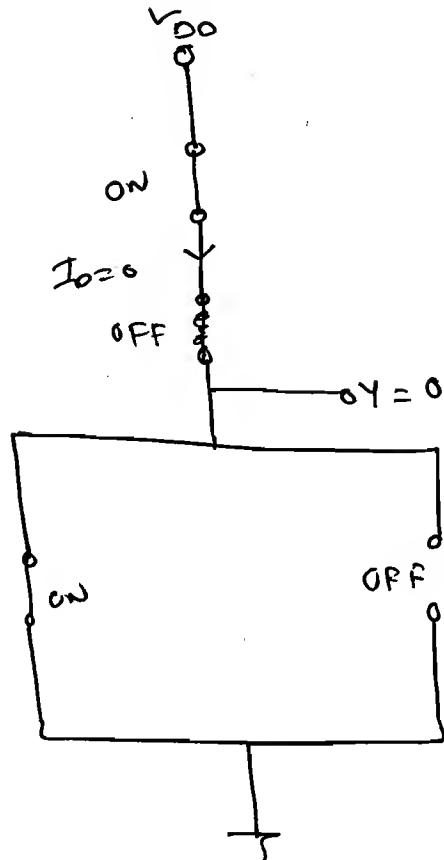
* 2 - input NOR Gate:



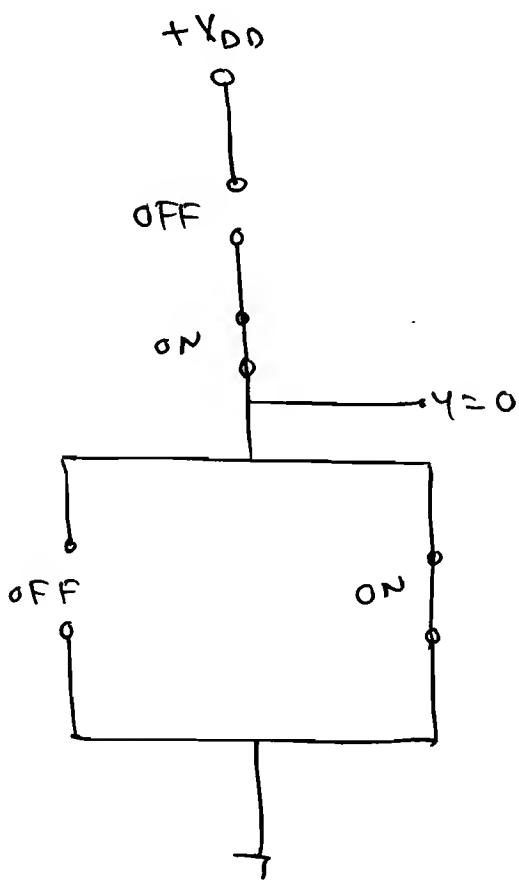
case - (i): $A=0, B=0$



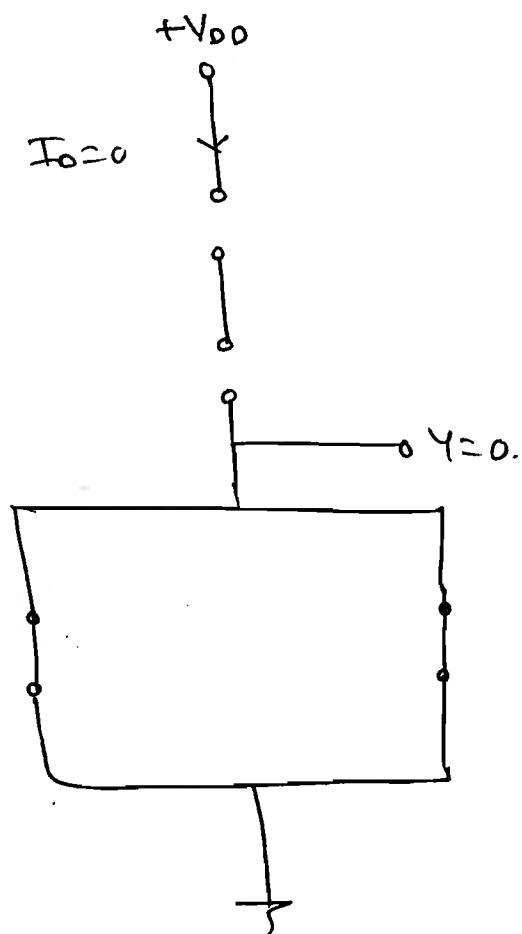
case - ii : $A=0, B=1$



case - (iii) : $A=1, B=0$



case - (iv) : $A=1, B=1$



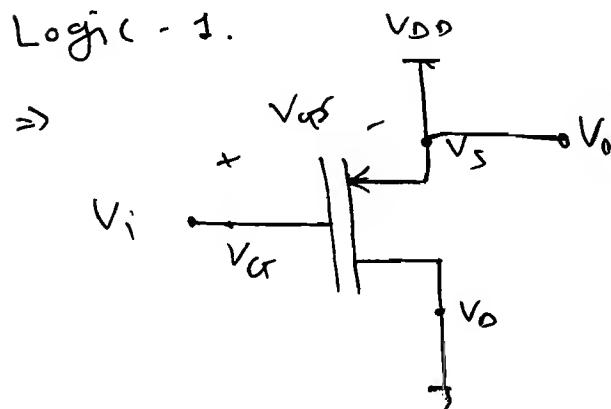
IMP Concept:

⇒ Why pmos is connected to ~~V_{DD}~~ & nmos is connected to ~~V_{SS}~~ in CMOS?

Ans:

⇒ PMOS Transistor passes Logic - 1 without distortion. But it passes Logic - 0 with distortion. Therefore PMOS transistors always connected to V_{DD} (or) pulled up to pass Logic - 1.

Logic - 1.



⇒ if $V_i = 0$. $\Rightarrow V_o$ should be V_{DD} (or).

i.e. PMOS is in ON state.

for that $V_{GS} < V_T$.

$$\text{let, } V_T = -0.7V.$$

$$\therefore V_{GS} - V_S < V_T.$$

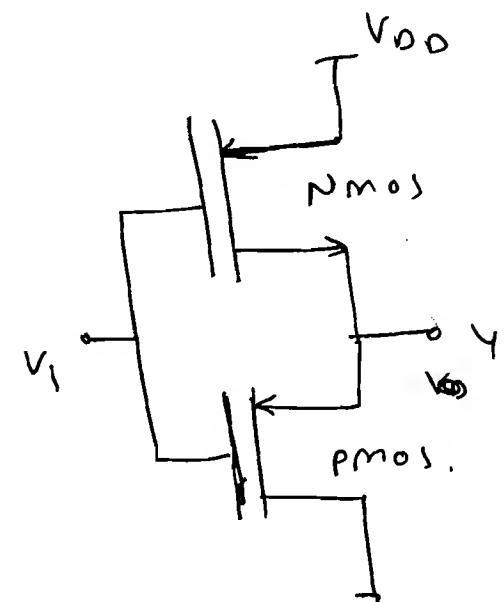
$$\therefore 0 - V_o < V_T.$$

$$\therefore V_o > -V_T.$$

$$\therefore |V_o| > |V_T|.$$

$$\text{i.e. } V_o > 0.7V.$$

So, instead of getting '0'.. we get 0.7. So, distortion will occur.



Now, Let, $V_i = +V_{DD}$. \Rightarrow PMOS is OFF and V_o should be $+V_{DD}$.

$$\therefore V_{GTS} = V_G - V_S$$

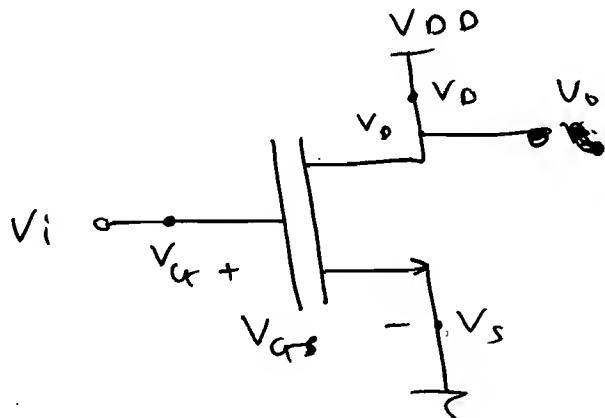
$$\therefore V_{GTS} = V_{DD} - V_{DD} = 0$$

$V_{GTS} = 0 \Rightarrow V_G \approx V_{DD}$. PMOS is OFF and $V_S = V_o = +V_{DD}$ perfect.

So, PMOS passes Logic '1' without distortion and passes Logic '0' with distortion.

\Rightarrow Nmos:

\rightarrow NMOS Transistor passes Logic - 0 without distortion and passes Logic - 1 with distortion. Therefore NMOS Transistor always connected to ground (or) pulled down to pass Logic - 0.



\Rightarrow In order to get $V_o = +V_{DD}$, $V_i = 0 \Rightarrow$ in ~~set~~ ^{Cut-off}.

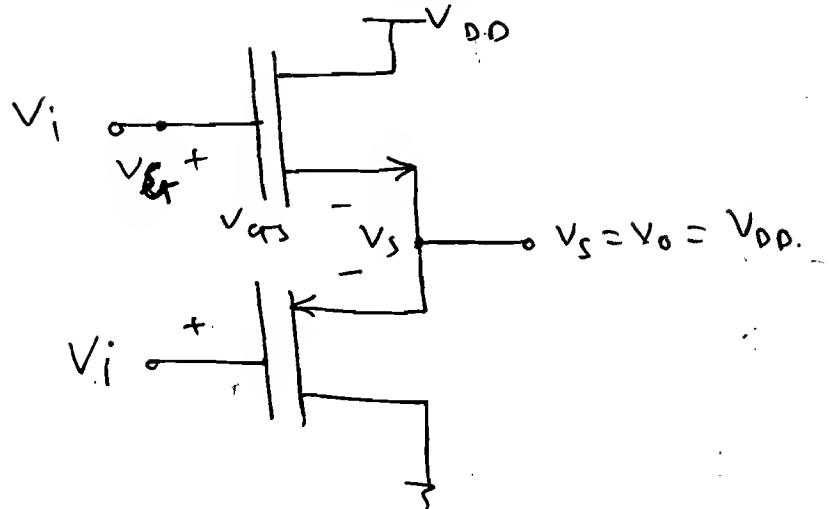
But for cut-off $V_{GTS} < V_T$. Let $V_T = 0.3V$

$$\therefore V_G - V_S < 0.3$$

$$\therefore V_G < 0.3$$

so, V_i should be > 0.3 .

71
 \Rightarrow Now, if NMOS is connected to up-side then,



\Rightarrow Now, if $V_i = 0$ then $V_s = V_0 = +V_{DD} = +5V$ for inverter.

in order to get $V_s = V_0 = +V_{DD} = +5V$ NMOS should be in cut off. So,

$$\therefore V_{DS} \ll V_T, \text{ let } V_T = 0.7V.$$

$$\therefore V_G - V_S \gg 0.7.$$

$$\therefore 0 - V_S \gg 0.7.$$

$$\therefore V_G \gg 0.7V. \quad \text{So, } -5 \gg 0.7 \rightarrow \text{not possible}$$

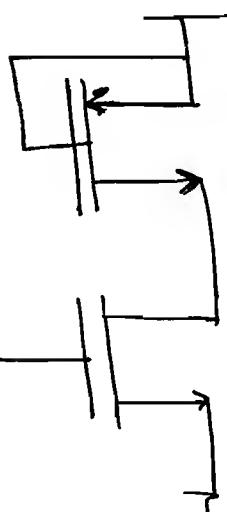
So, we get ~~$V_0 = 0$~~ instead of ~~$V_0 = 5V$~~ .

So, we get distortion. NMOS is OFF.

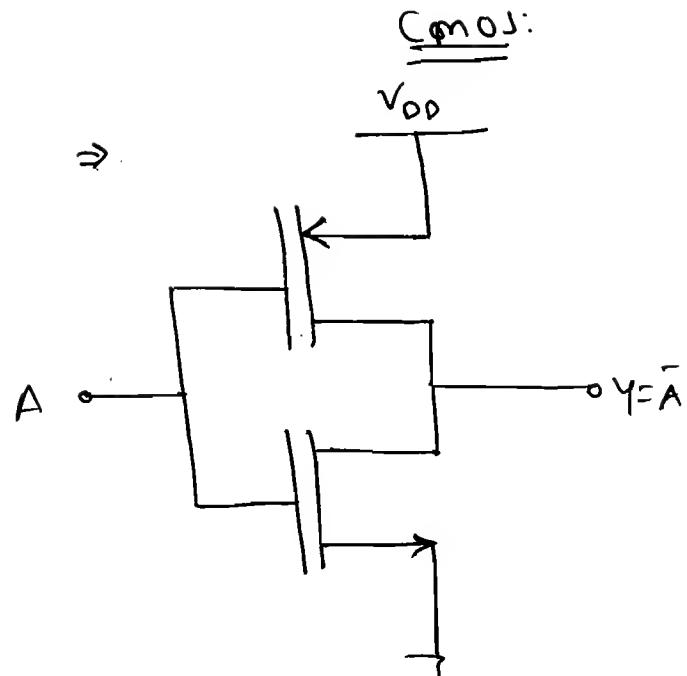
\Rightarrow So, NMOS Transistor passes Logic-0 without distortion. But if passes Logic-1 with distortion. Therefore NMOS Transistor always connected to ground (or) pulled down to pass Logic-0.

★ Inverter:

n-MOS

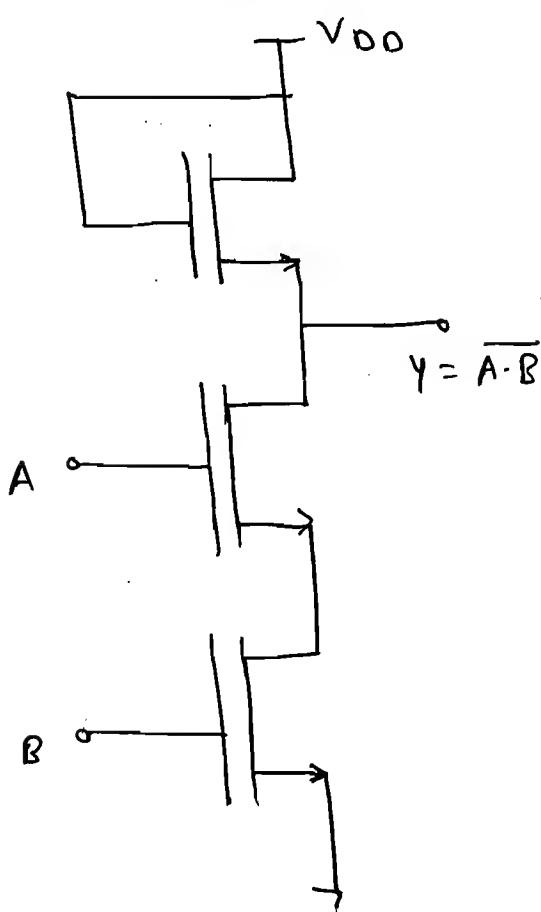


CMOS:

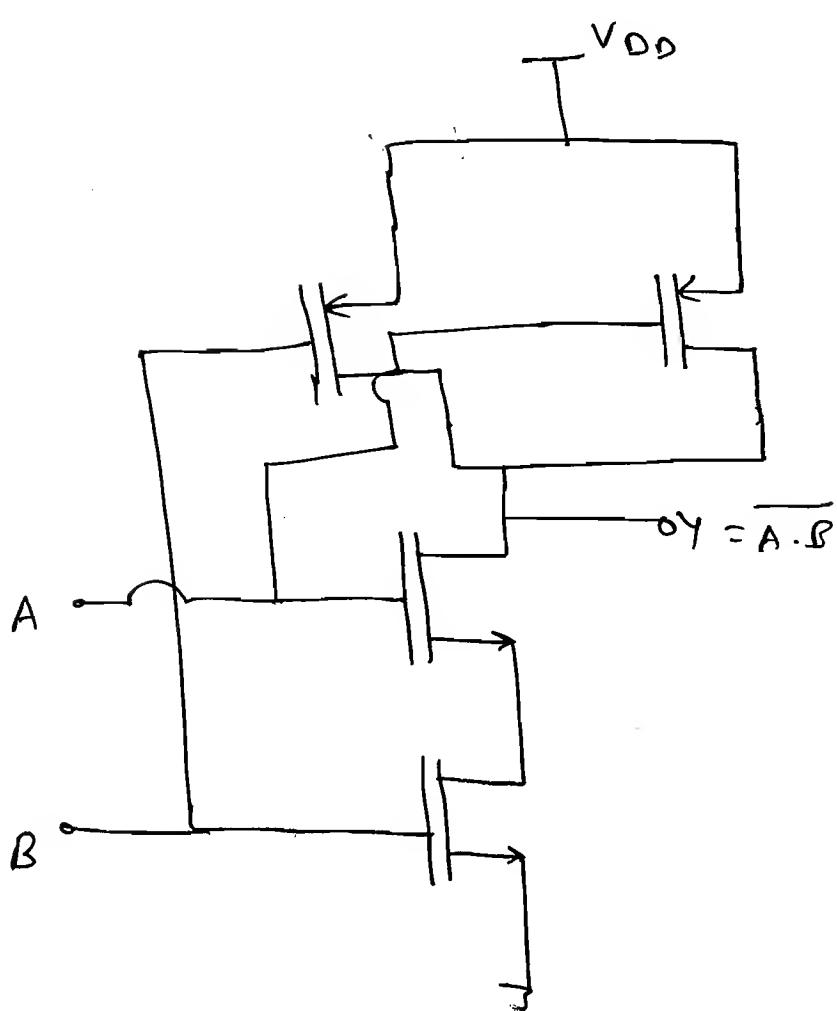


★ 2 input NAND gate:

n-MOS

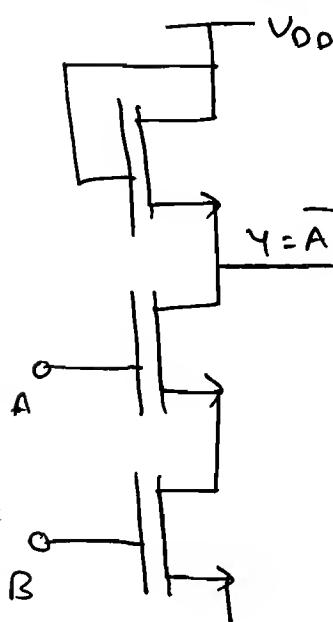


CMOS:

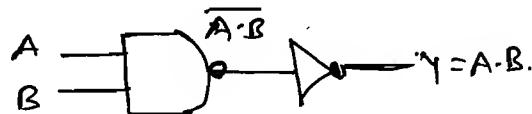


* 2-Input AND Gate:

Nmos



NAND

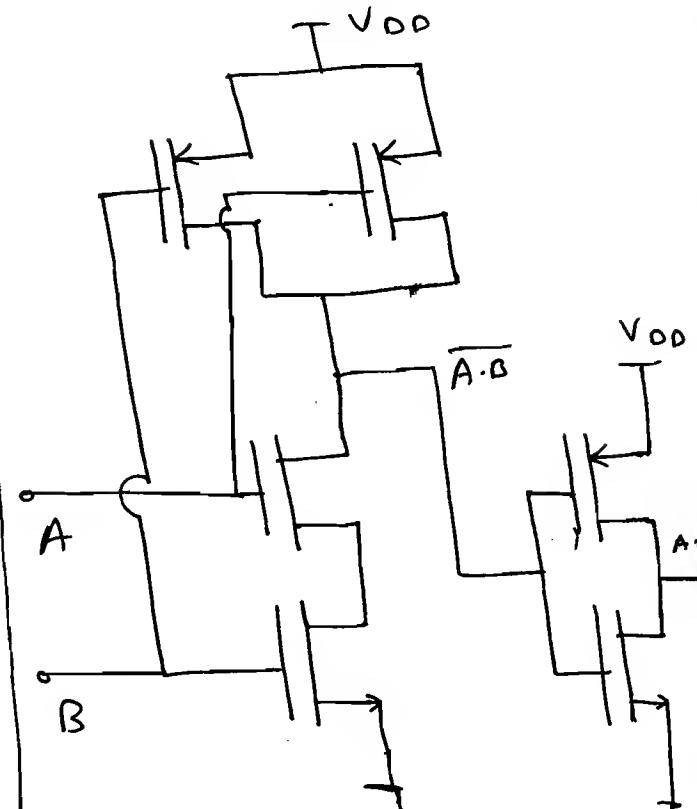


V_{DD}

$Y = \overline{A \cdot B}$
 $Y = A \cdot \overline{B}$

NOT

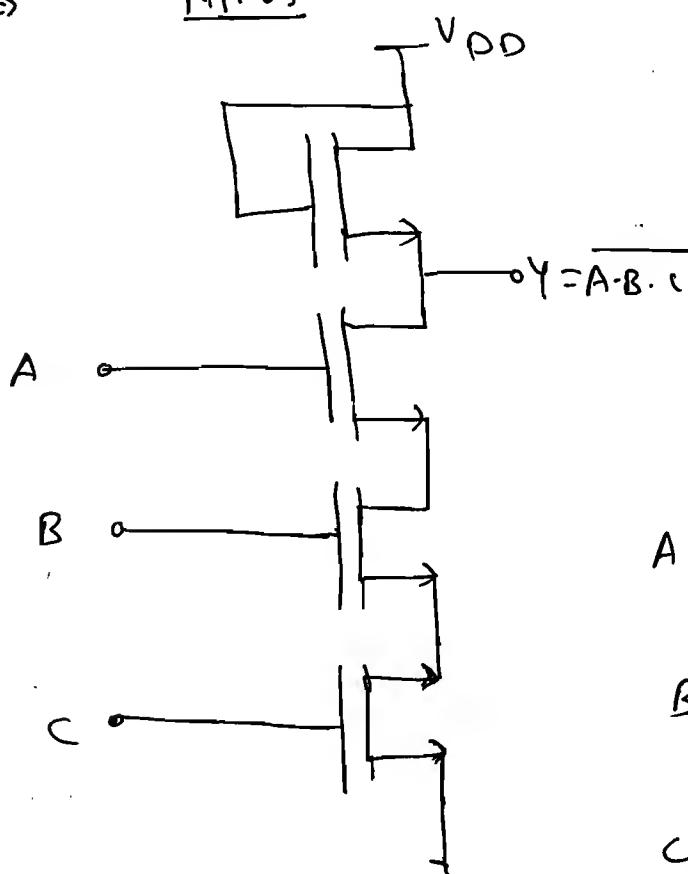
CMOS:



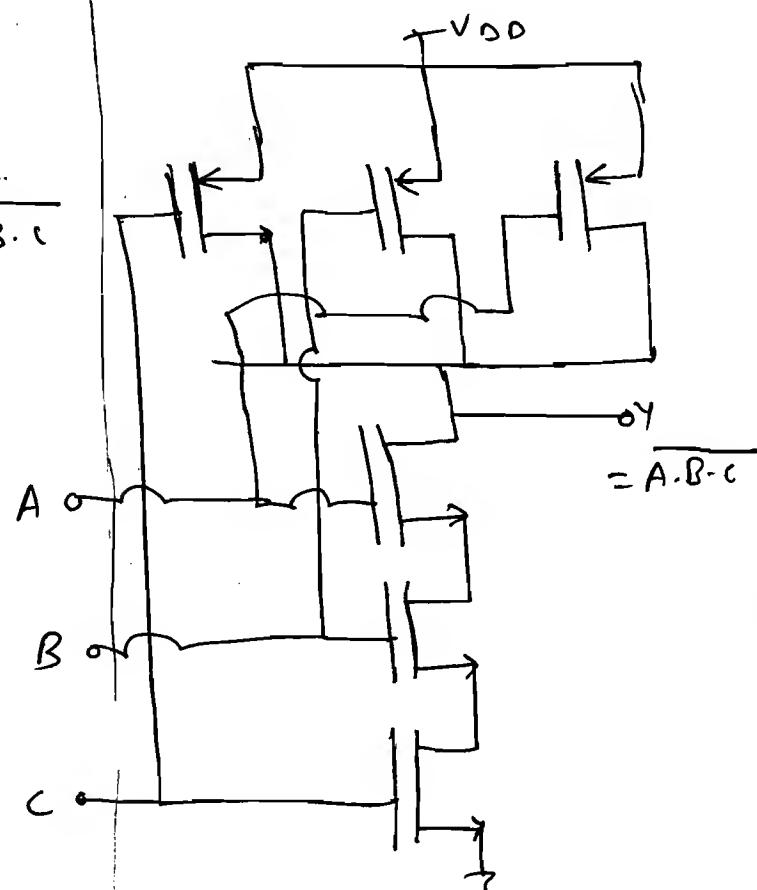
* 3-Input NAND Gate:

⇒

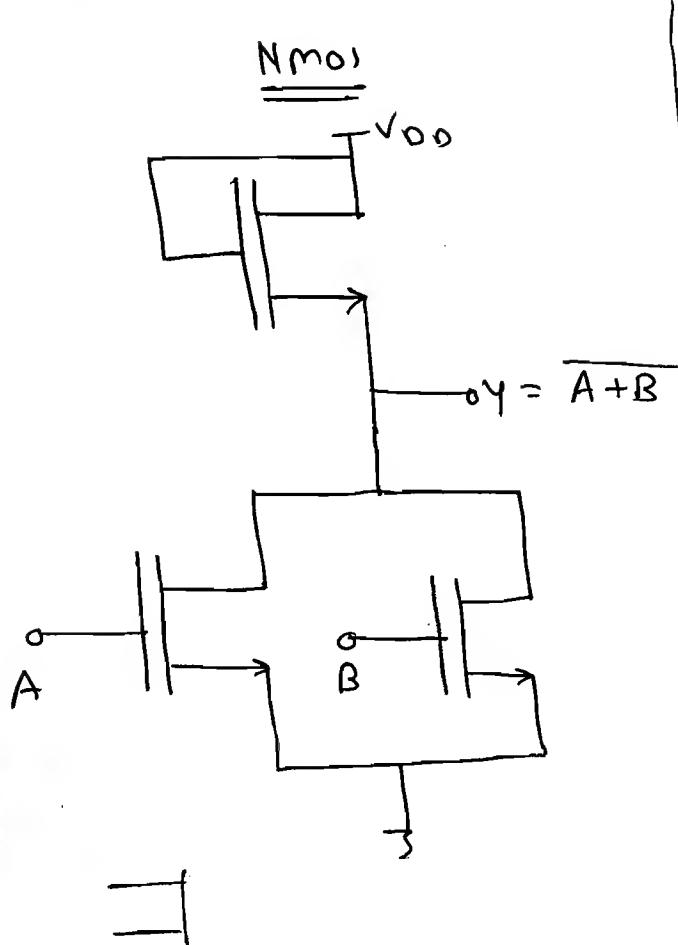
Nmos:



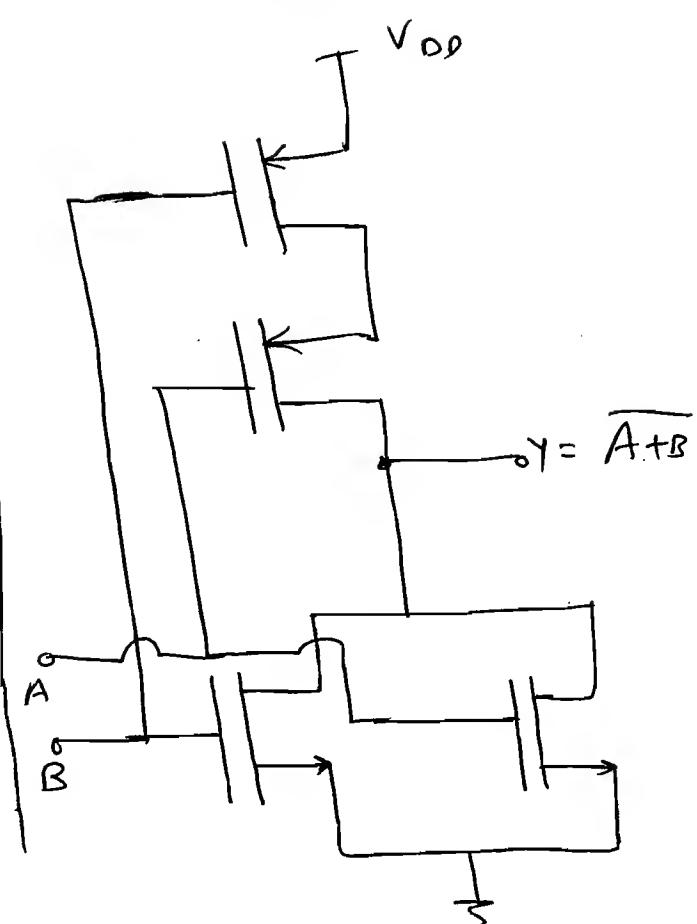
CMOS



* 2 input NOR gate:

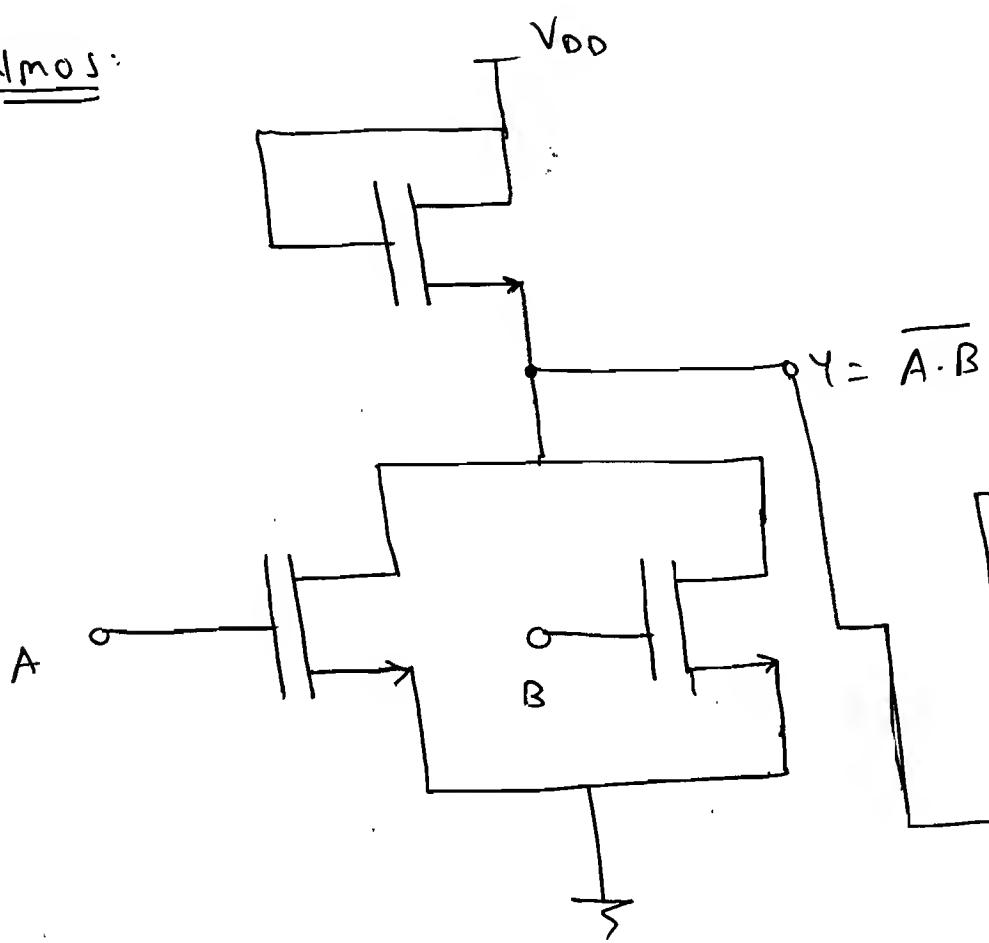


Cmos

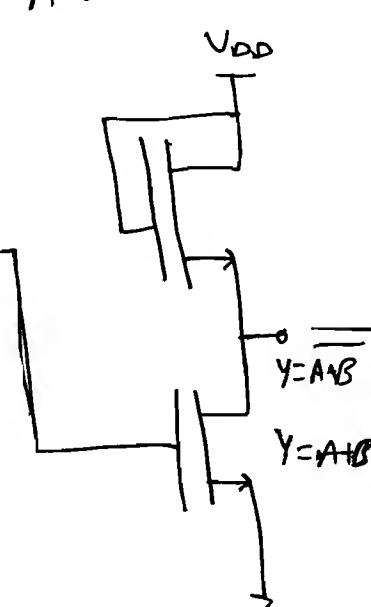


* 2 input OR gate:

Nmos:



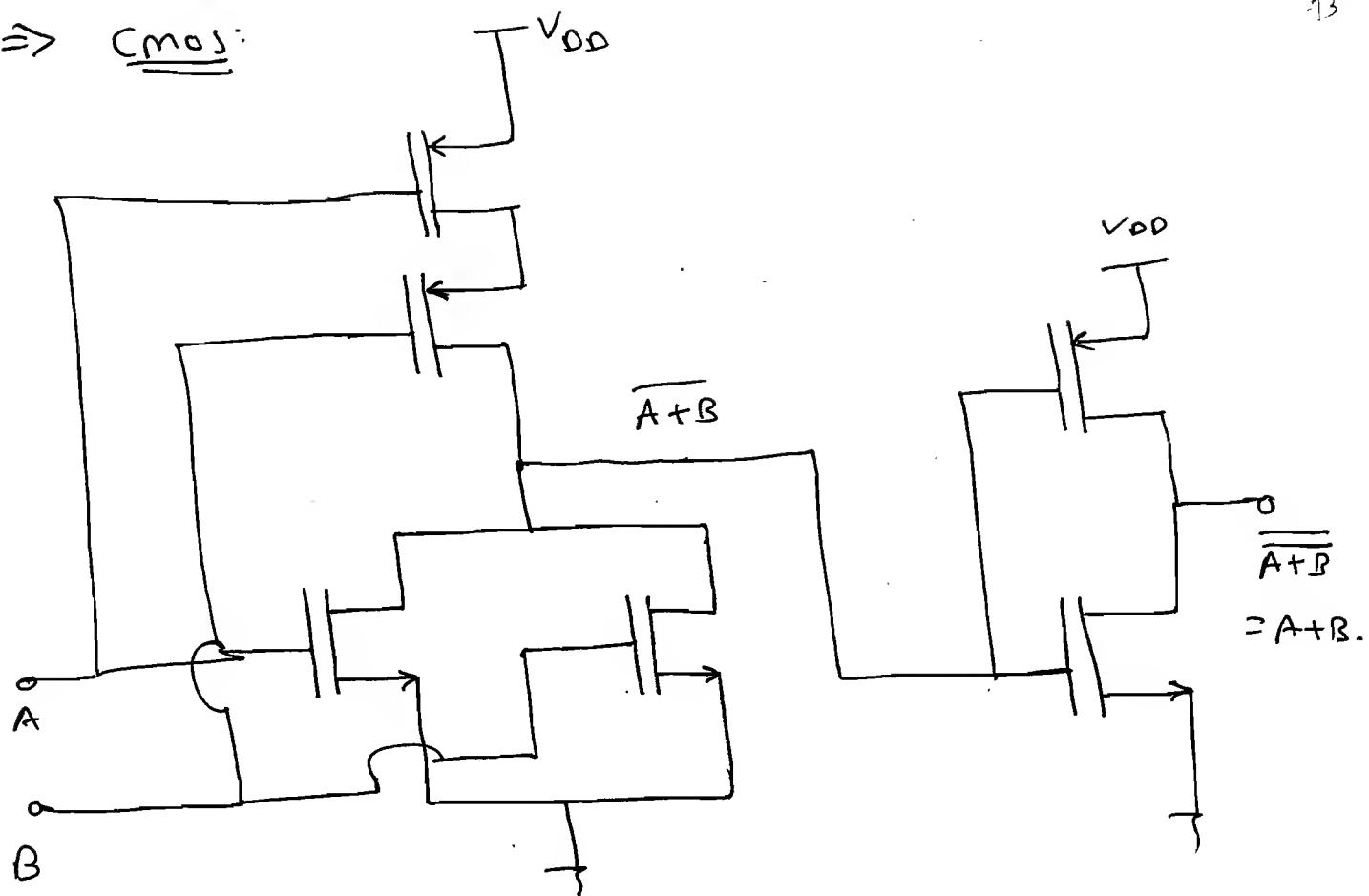
V_{DD}



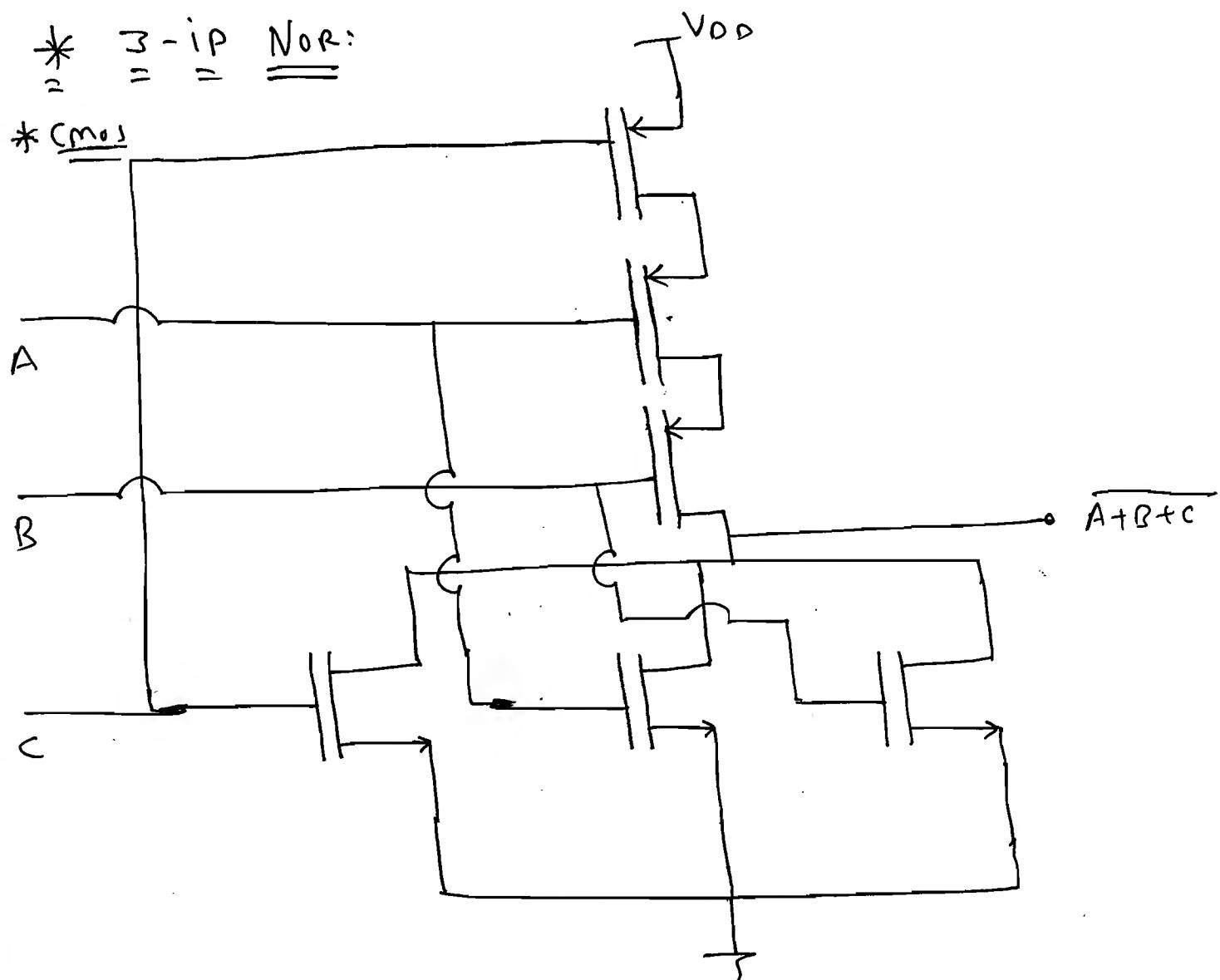
$Y = A \cdot B$

$Y = A+B$

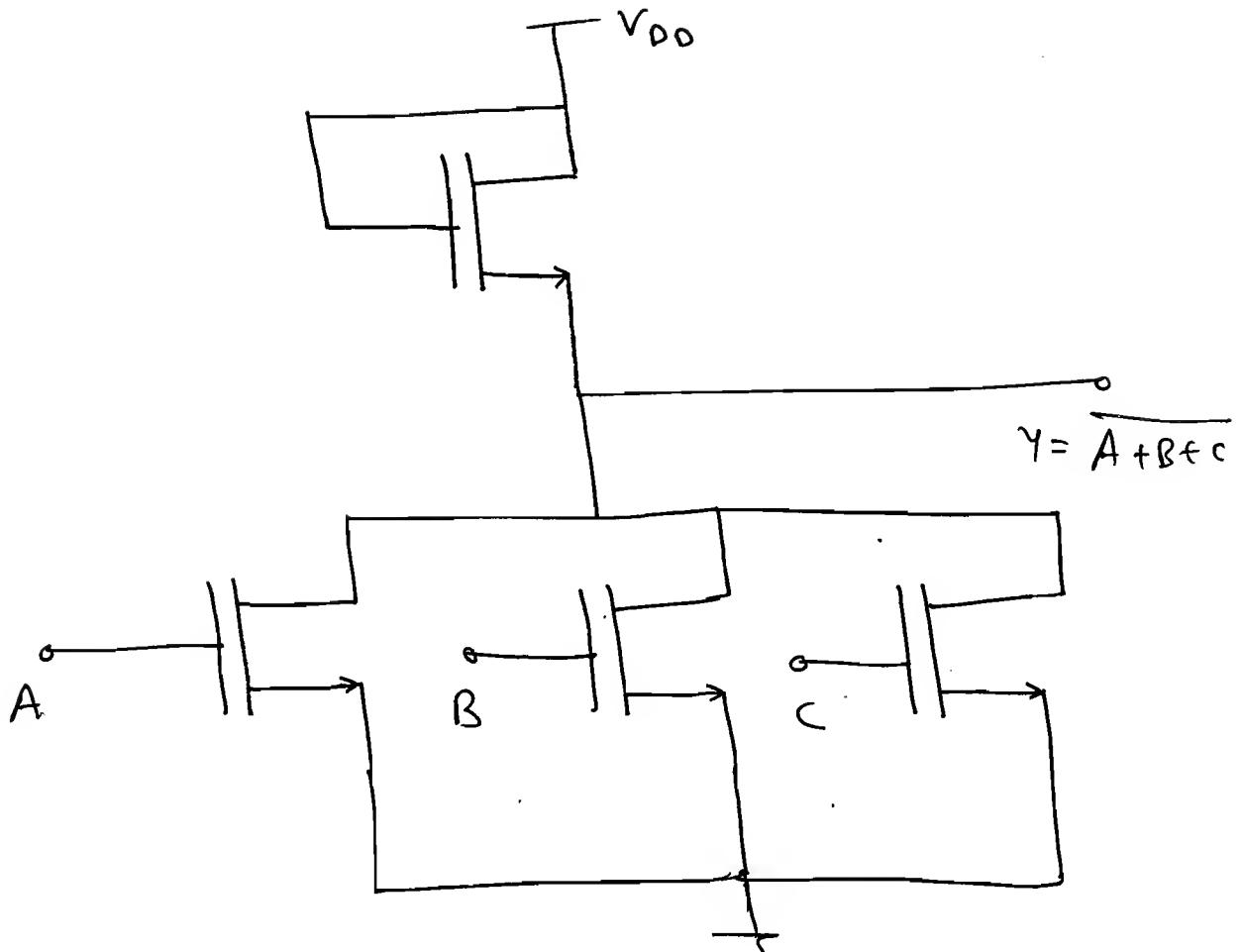
⇒ Cmos:



* \Rightarrow 3 - iP NOR:



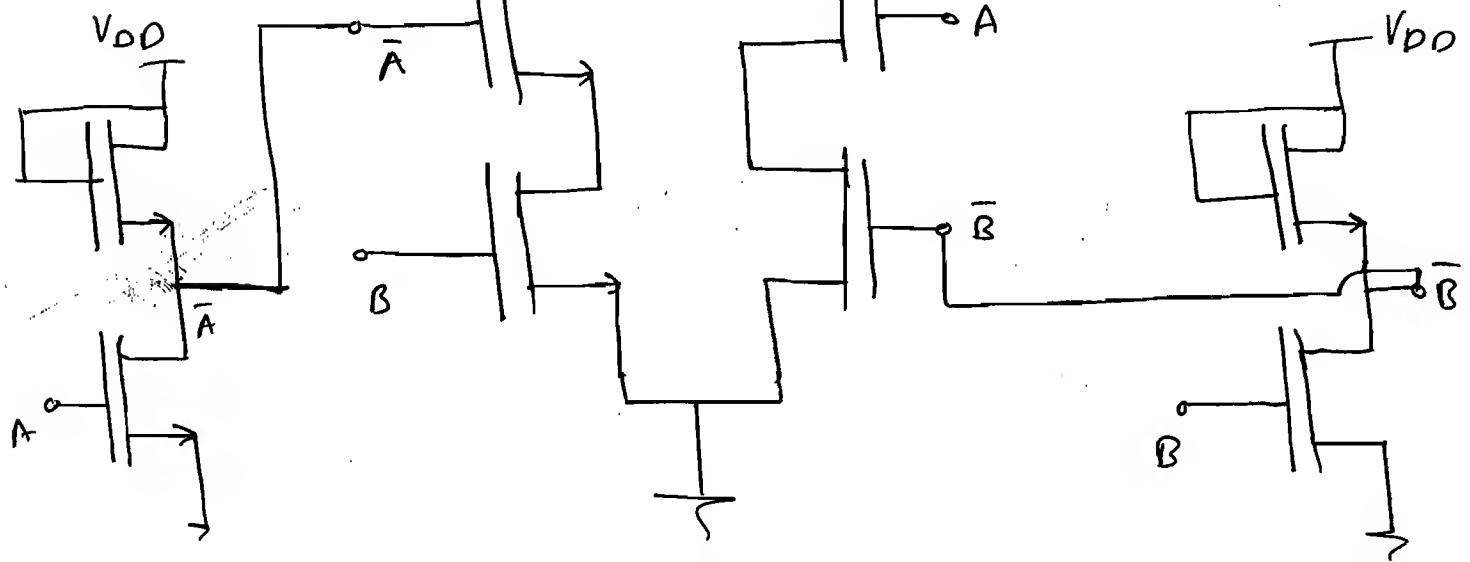
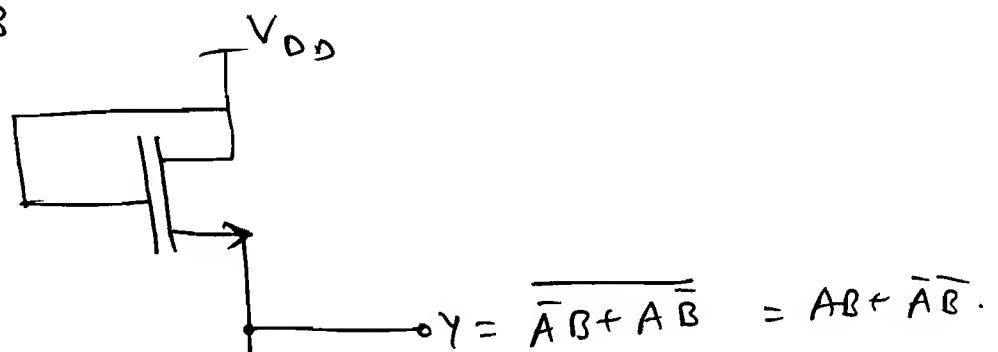
* NMOS:



* 2-Input XNOR gate:

$$Y = A \odot B = \overline{\bar{A}B + A\bar{B}}$$

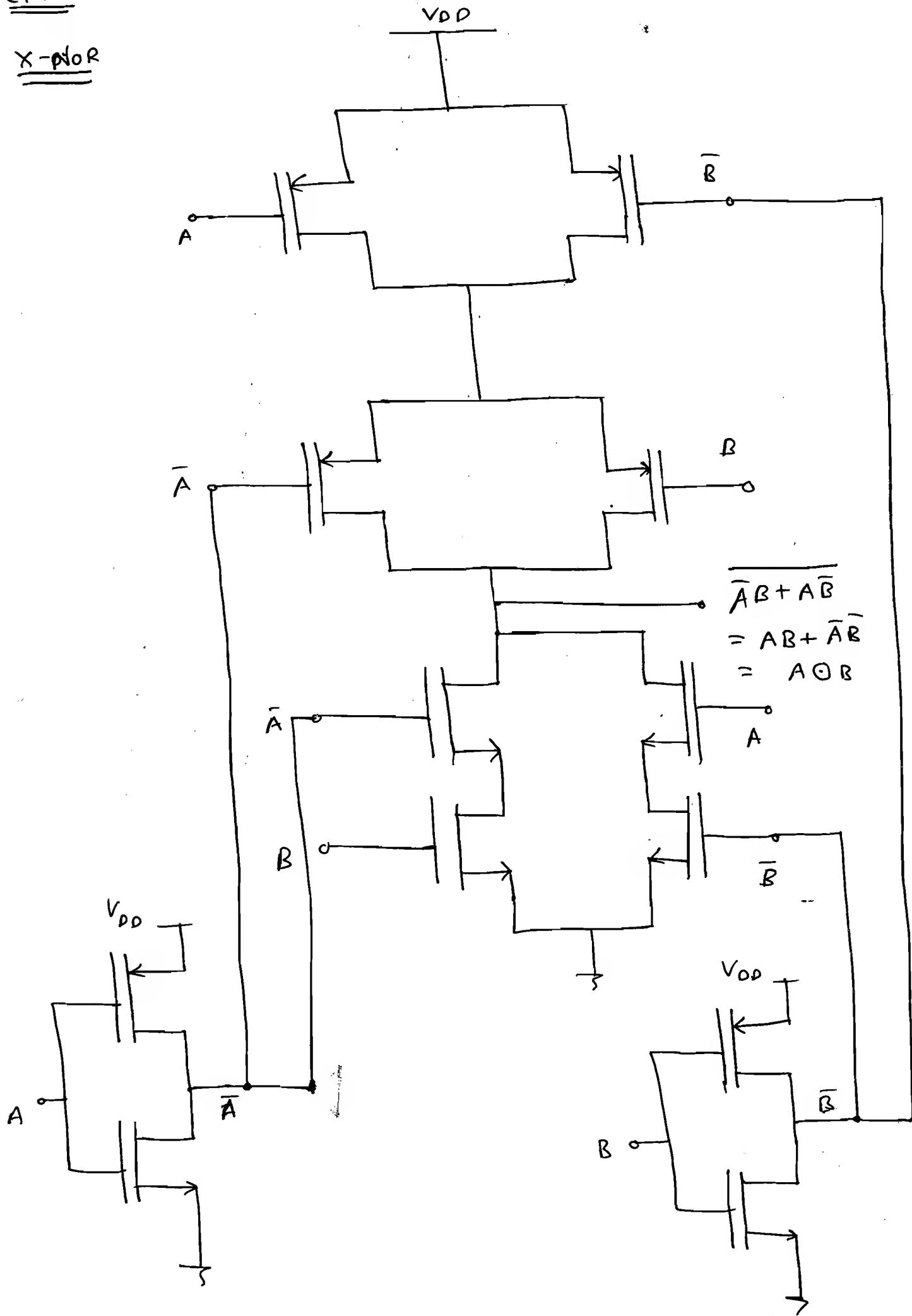
$$Y = AB + \bar{A}\bar{B}$$



CMOS

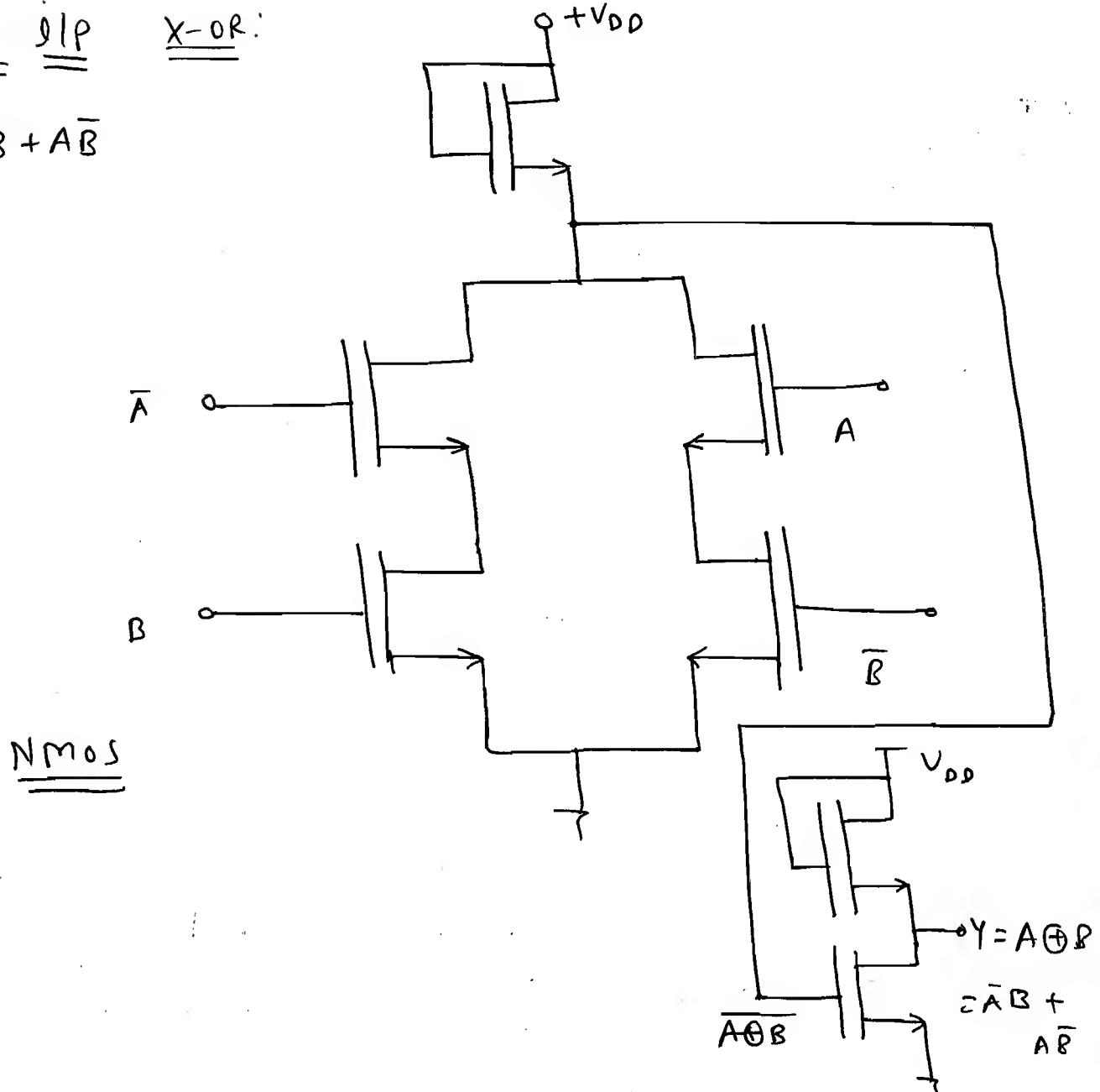
74

X-OR



* 2 g/p X-OR:

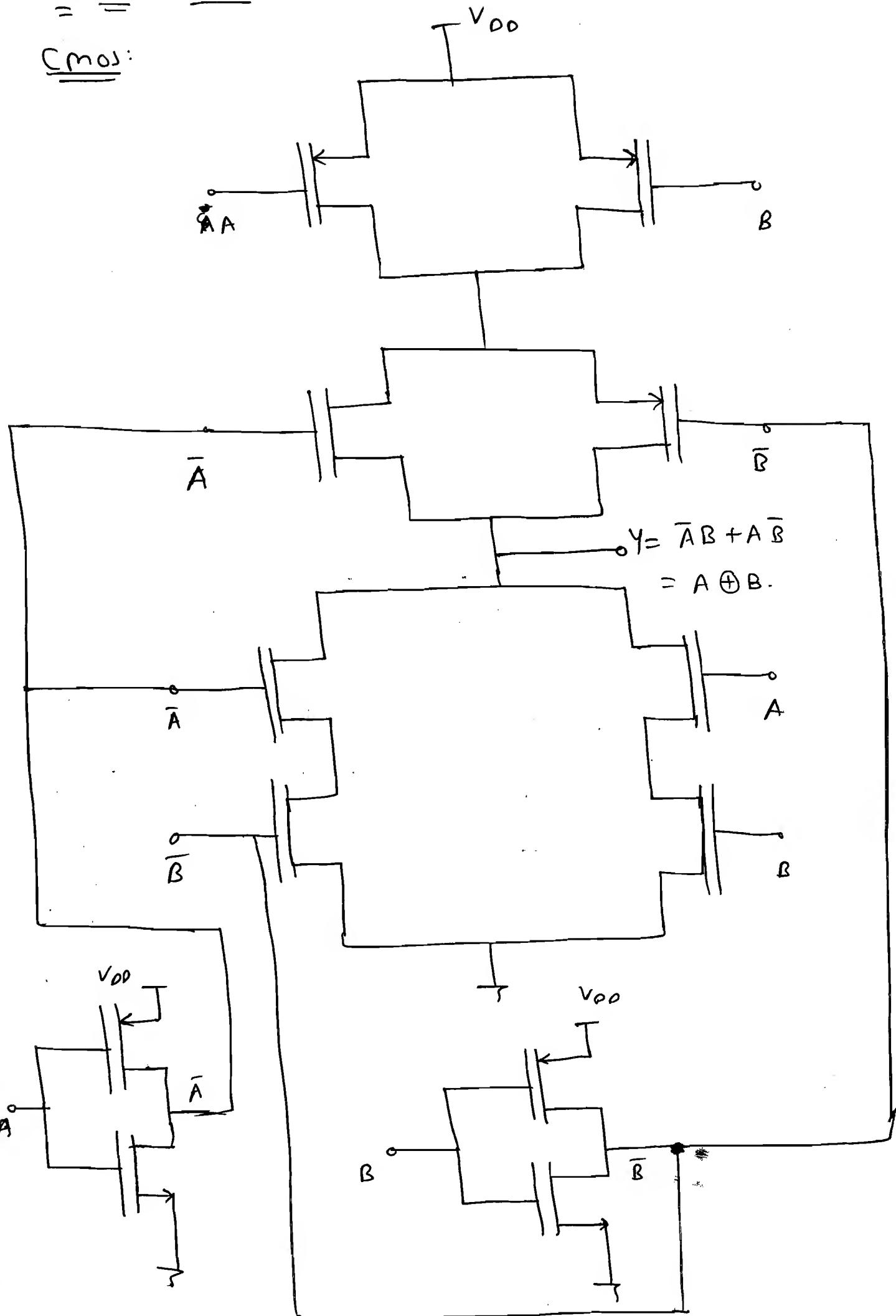
$$Y = \bar{A}B + A\bar{B}$$



$$* \underline{d - ilp} \quad \underline{x - or} :$$

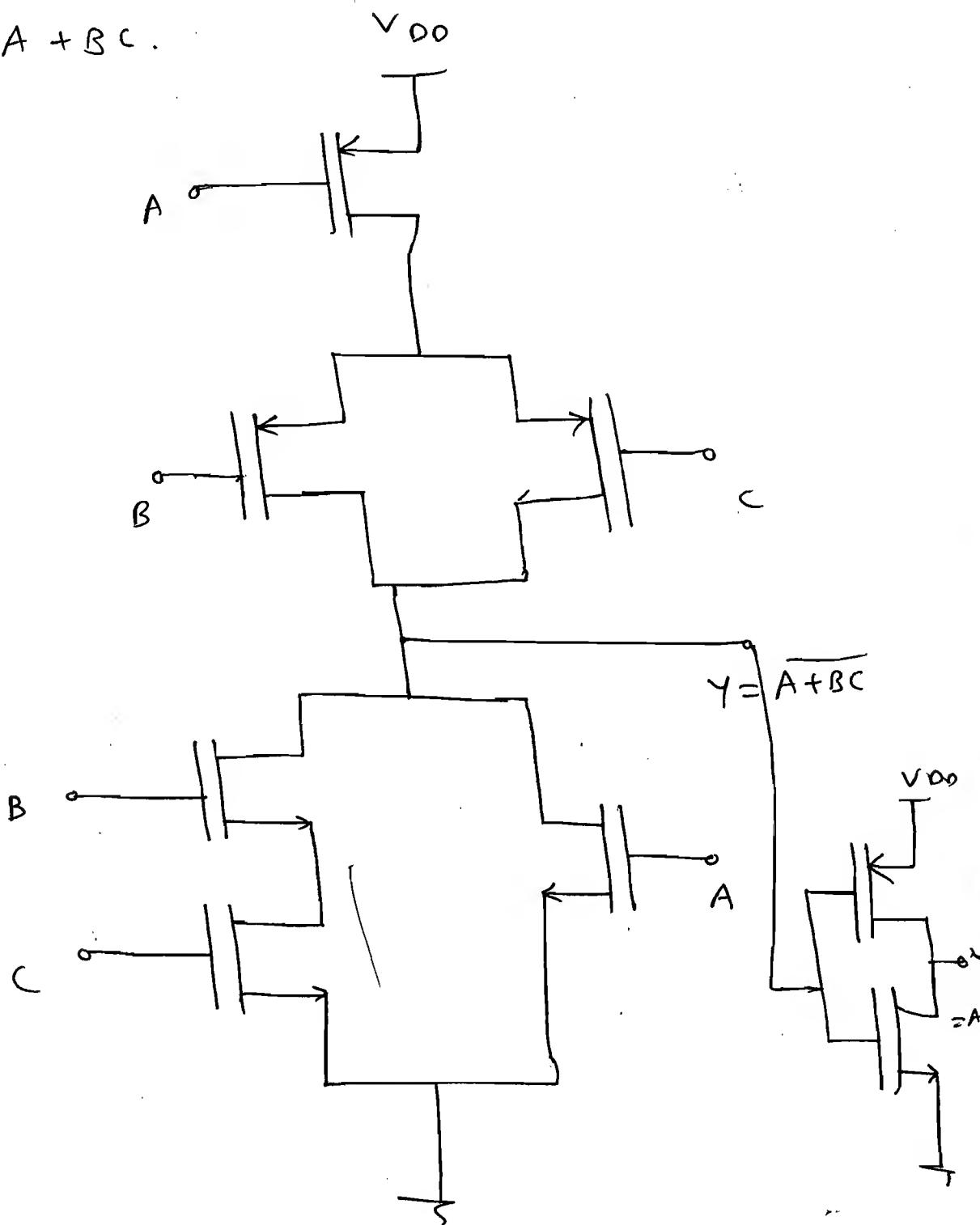
75

Cmos:



* Implement the following in CMOS technology:

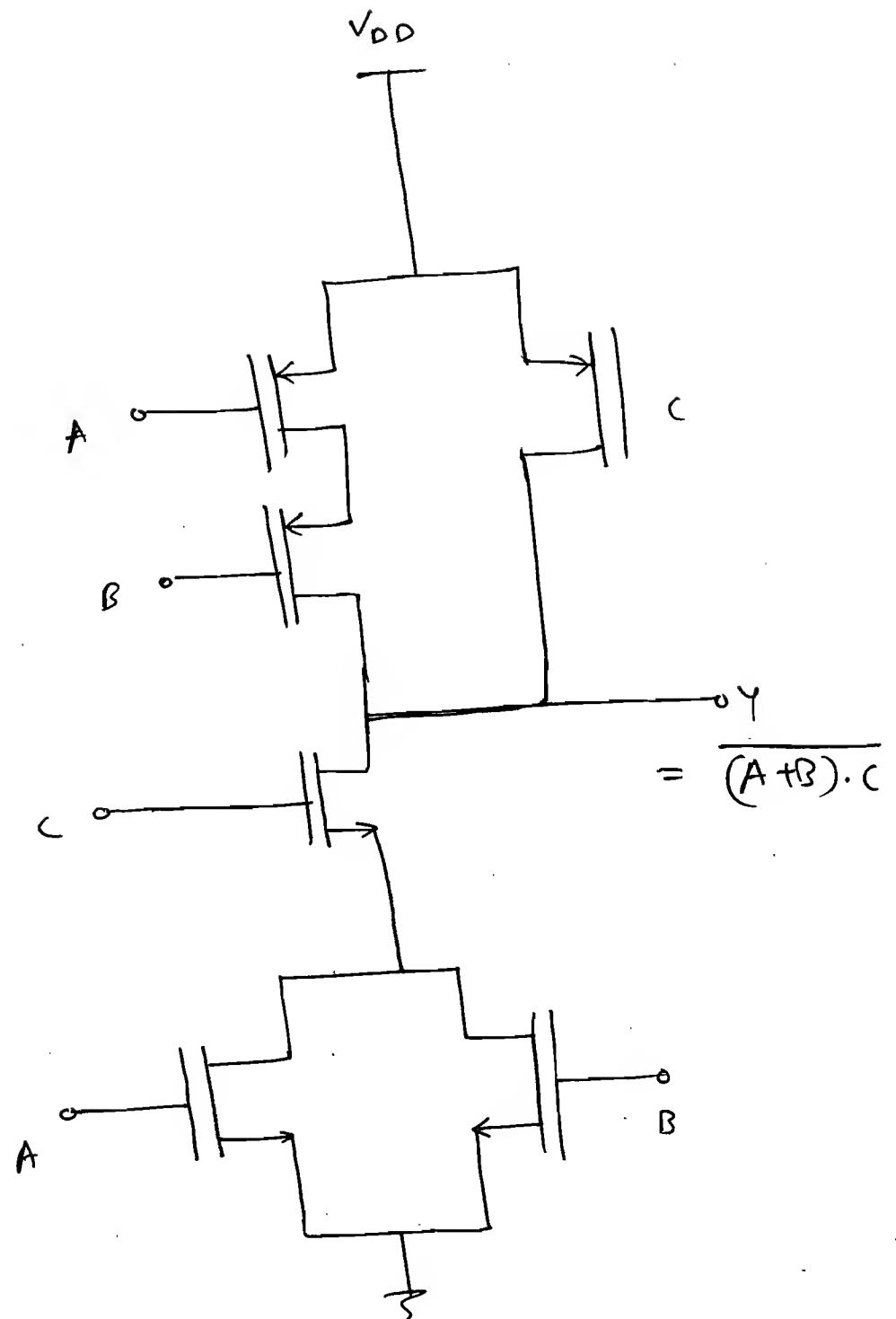
① $Y = A + BC$.



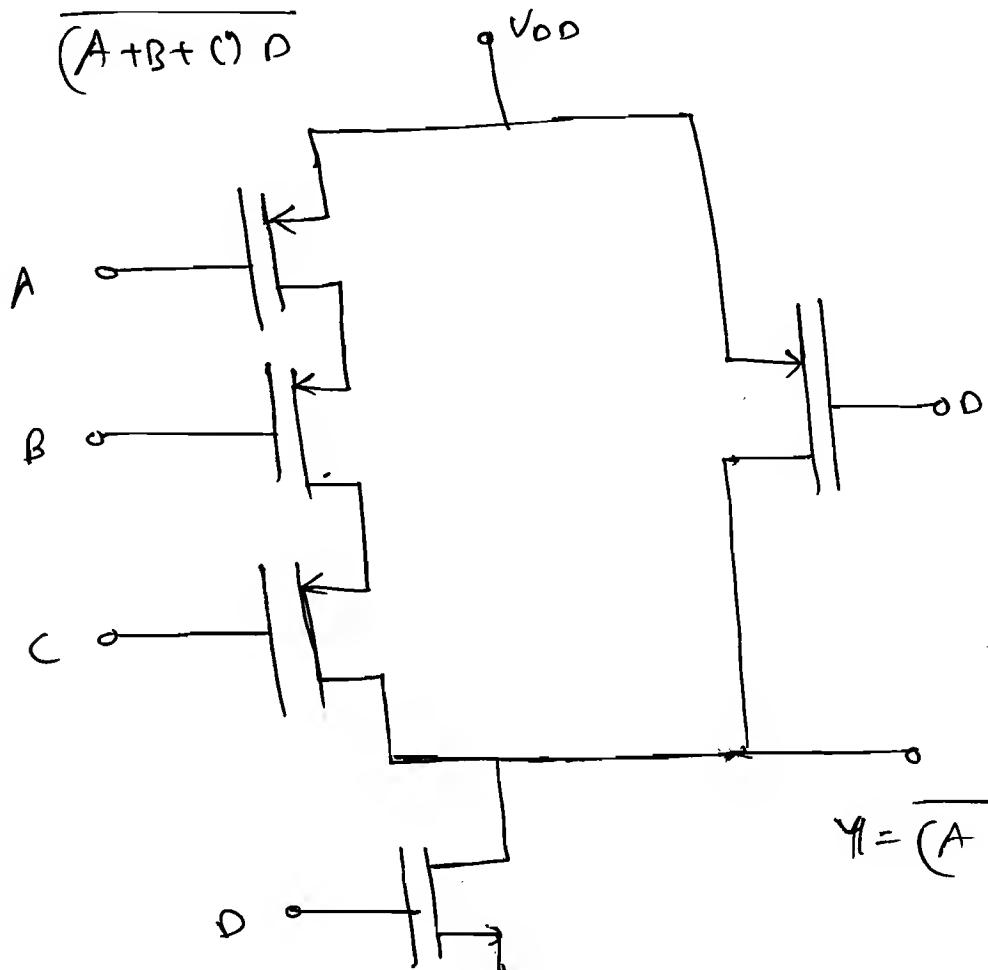
② $Y = \overline{(A+B)} \cdot C$

\Rightarrow

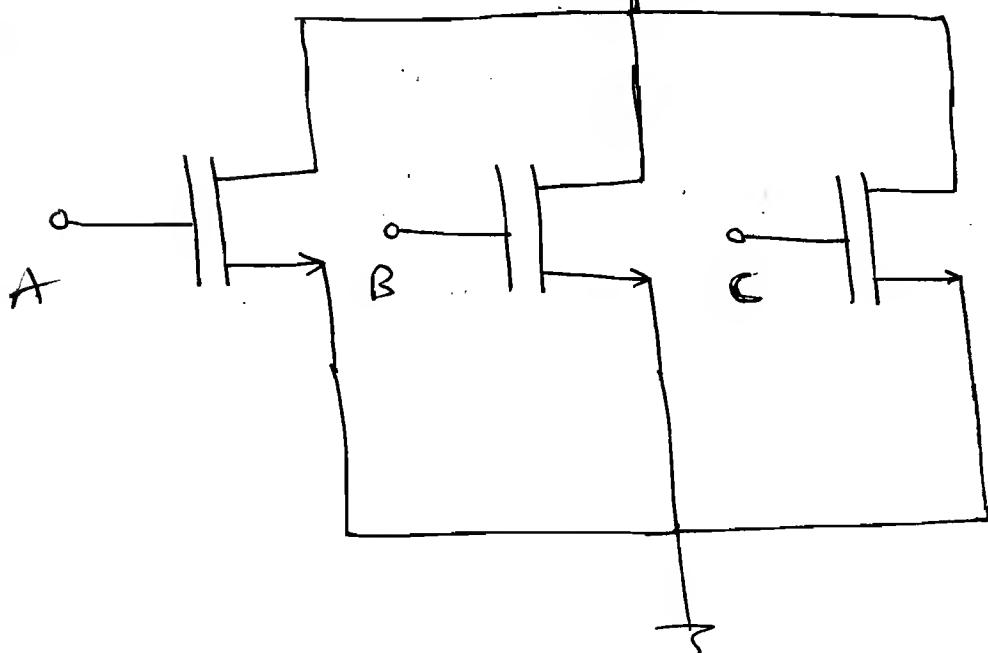
16



$$3. Y = \overline{(A+B+C)D}$$

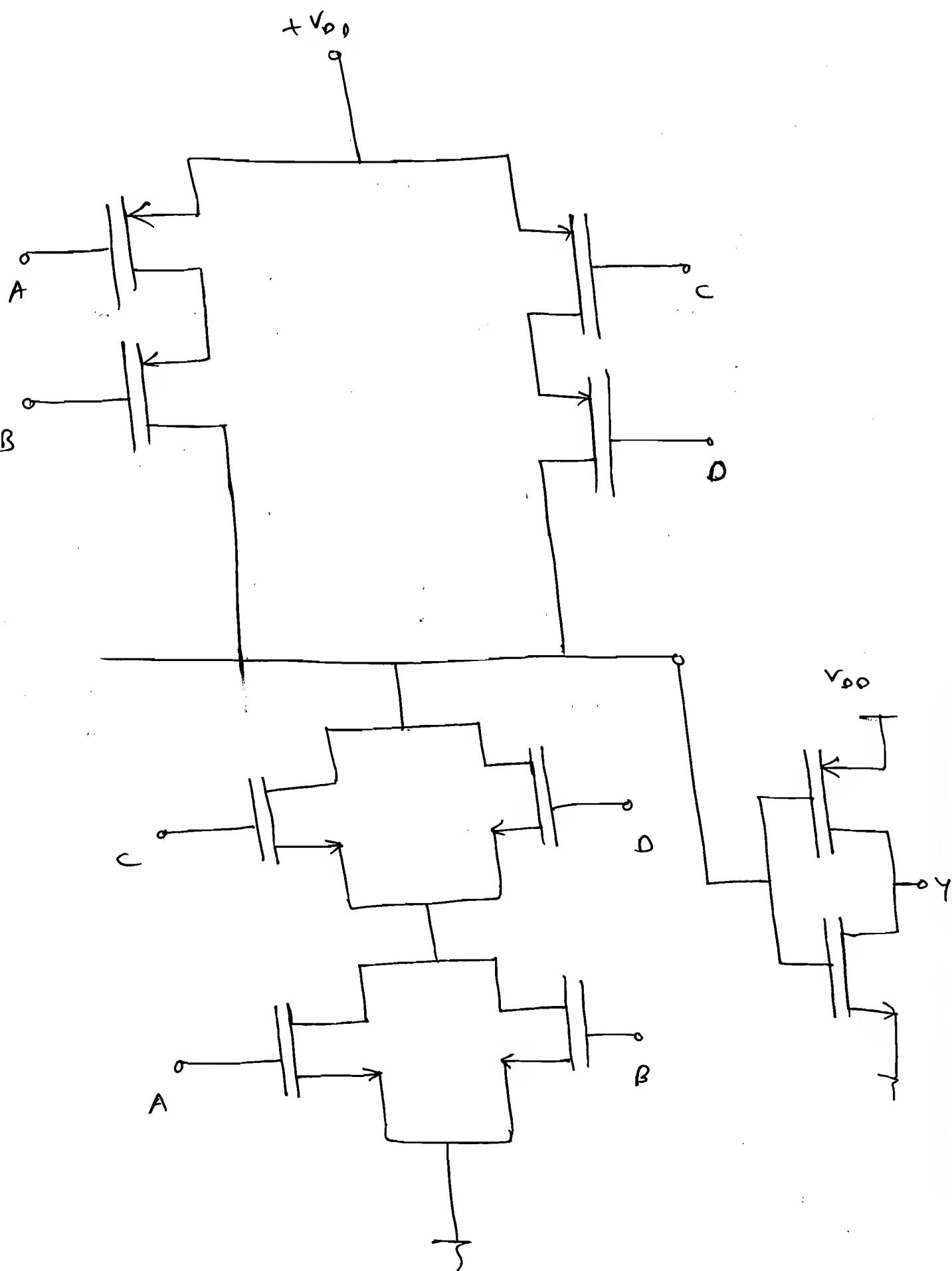


$$Y = \overline{(A+B+C)D}$$

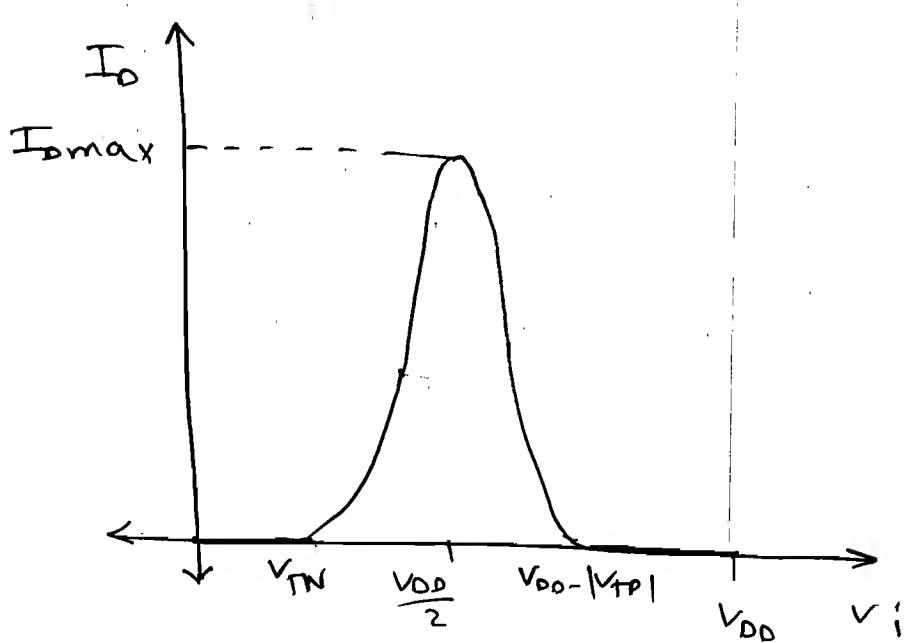
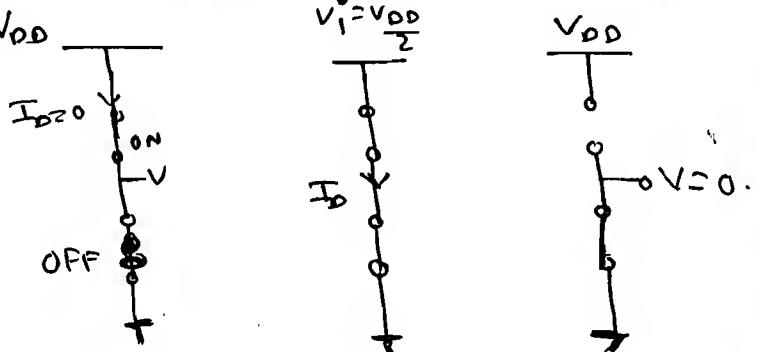
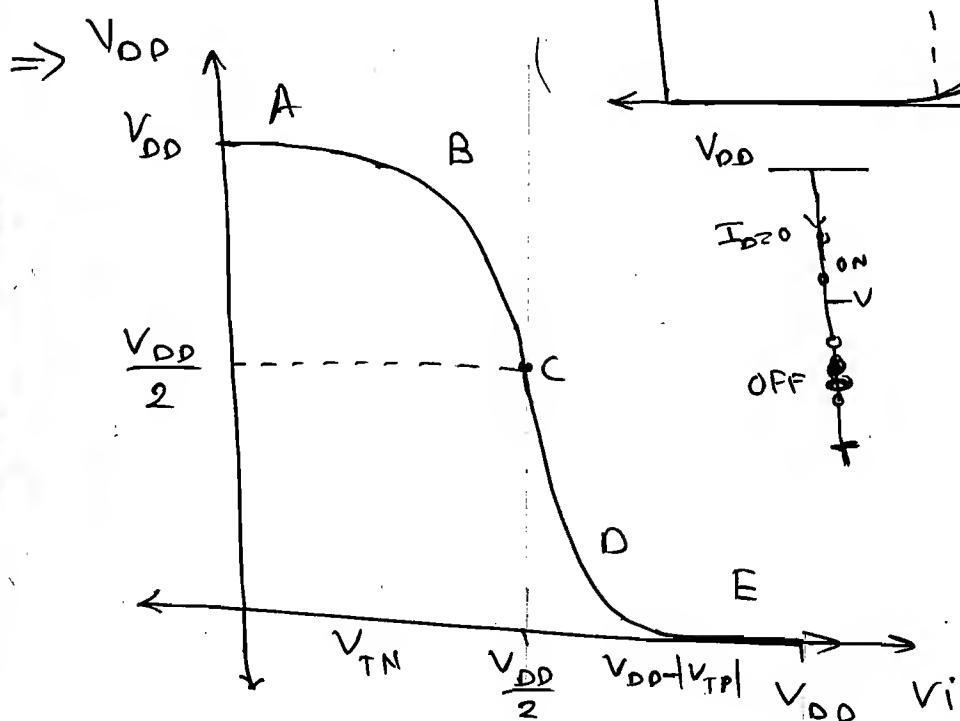
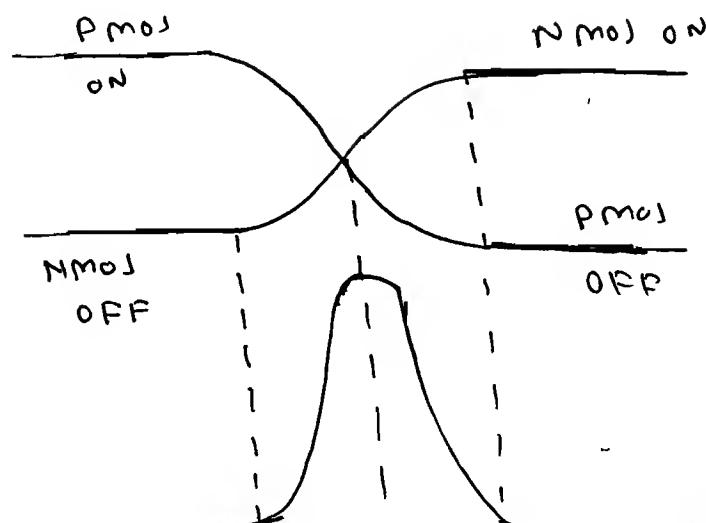
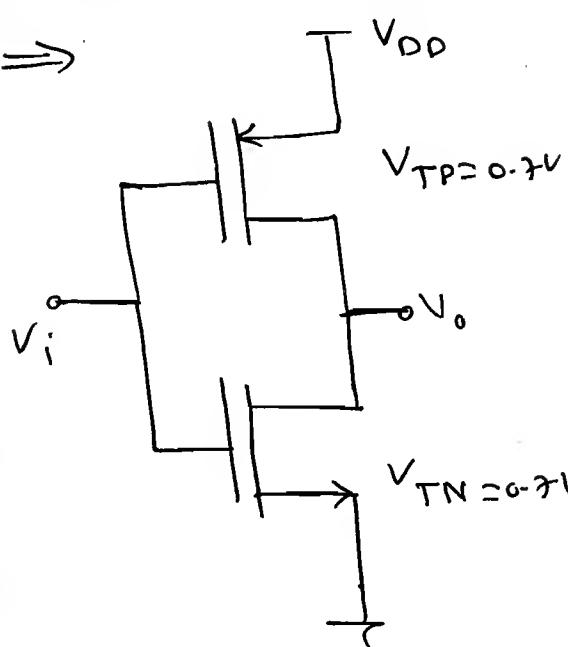


$$4. Y = (A+B)(C+D)$$

11



★ Transfer characteristics of an inverter



Reg	Condition	PMOS	NMOS	Output
A	$0 < V_i < V_{TN}$	Linéaire	Cut-off	$V_o = V_{DD}$
B	$V_{TN} < V_i < V_{DD}/2$	Linéaire	Sat	$V_o > \frac{V_{DD}}{2}$
C	$V_i = V_{DD}/2$	Sat	Sat	$V_o = \cancel{V_{DD}}$ does shorting
D	$\frac{V_{DD}}{2} < V_i < V_{DD} - V_{TP} $	Sat	Linéaire	$V_o < V_{DD}/2$
E	$V_i > V_{DD} - V_{TP} $	Cut-off	Linéaire	$V_o = 0$

$$\textcircled{1} \quad 0 < V_i < V_{TN}, \therefore$$

$$\Rightarrow V_i = \frac{V_{DD}}{2} \quad \text{NMOS}$$

PMOS

$$V_i = 0.5V$$

$$V_{GTS} = V_G - V_S$$

$$V_{GTS} = V_G - V_S$$

$$V_{GTS} = 0.5$$

$$= 0.5 - 5 = -4.5$$

$$V_{GTS} = 0.5 < (V_{TN} = 0.2V)$$

$$\therefore V_{GTS} = -4.5 < V_{TN}.$$

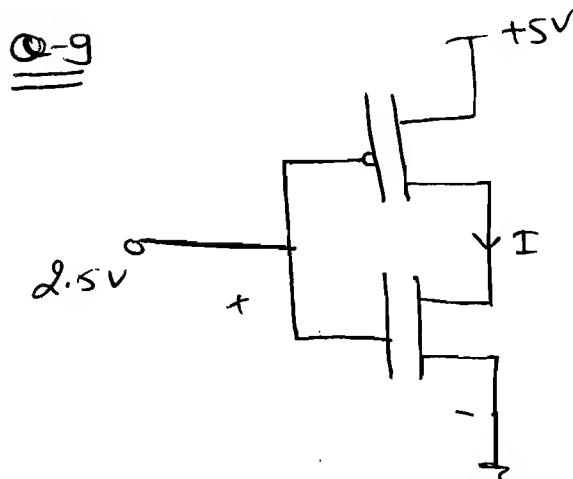
So, OFF

$$\text{Now, } V_{DS} = V_D - V_S$$

$$= V_{DD} - V_{DD} = 0$$

$$V_{DS} = 0. \quad V_{DS} - V_T = -4.5 - (-0.2) = -3.8 < V_{DS}.$$

$$V_{DS} > V_{GTS} - V_T \Rightarrow \text{linear.}$$



$$K_n = K_p = \mu_n C_{ox} \cdot \frac{W_n}{L_n}$$

$$= \mu_p C_{ox} \cdot \frac{W_p}{L_p} = 40 \text{ mA/V}^2$$

$$V_{GTS} = 2.5V$$

$$V_T = 1.1V$$

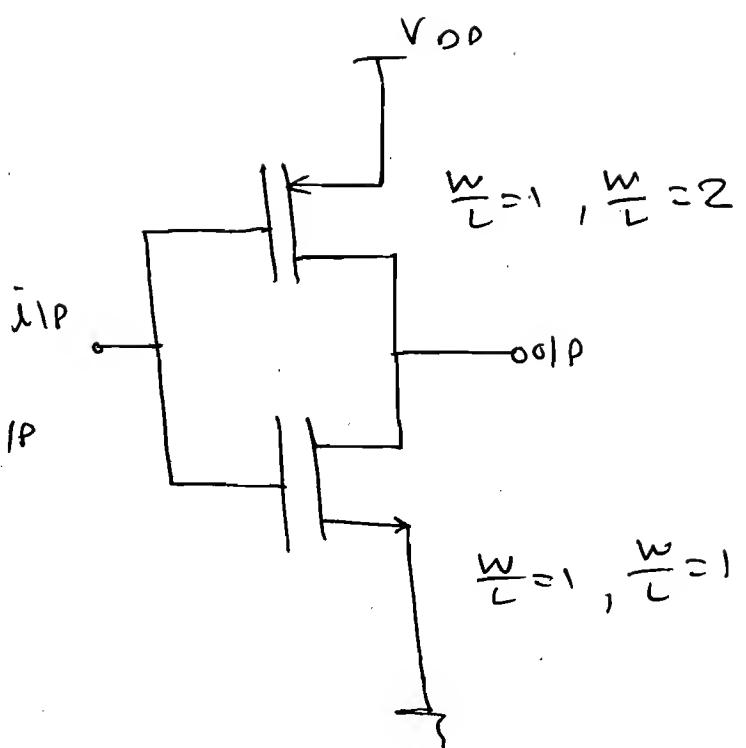
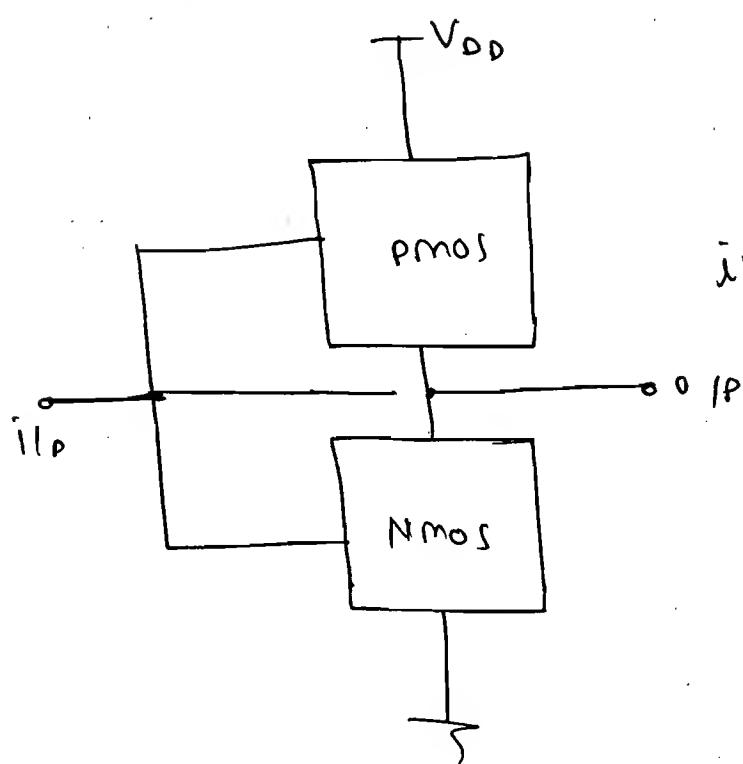
Soln.

$$I_D = \frac{1}{2} \mu_n C_{ox} \cdot \frac{W_n}{L_n} [V_{GTS} - V_T]^2$$

$$= \frac{1}{2} \times 40 \times 10^{-6} [2.5 - 1]^2 = 20 \times 10^{-6} \times 2.25$$

$$I = 45 \mu A$$

* Transistor Sizing:



n-mos

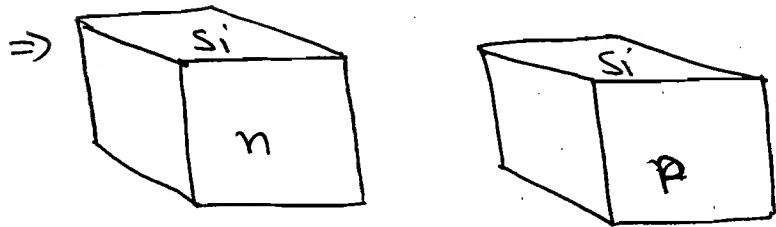
$$L = 1 \mu\text{m}$$

$$w = 1 \mu\text{m}$$

PMOS

$$L = 1 \mu\text{m}$$

$$w = 1 \mu\text{m}$$



$$\sigma_n = \mu_n \mu_n \tau$$

$$\sigma_p = \mu_p \mu_p \tau$$

$$\frac{\sigma_n}{\sigma_p} = \frac{\mu_n}{\mu_p} = \frac{1300}{500} \text{ cm}^2/\text{V-s}$$

$$\mu_p = 500 \text{ cm}^2/\text{V-s}$$

$$\therefore \mu_n \approx 2 \mu_p$$

$$\therefore \mu_n \approx 2 \mu_p$$

$$\Rightarrow \sigma_n = 2 \sigma_p$$

$$\therefore \sigma_p = 2 \sigma_n$$

$$\therefore R_p = \frac{\sigma_p L}{A}$$

$$\downarrow R_p = \frac{\sigma_p L}{A}$$

$$\therefore R_p = 2 R_n$$

$$\text{for } R_p = R_n$$

$$\therefore A_p = 2 A_n$$

$$\Rightarrow T\left(\frac{w}{l}\right)_p = 2\left(\frac{w}{l}\right)_n$$

$\Rightarrow \underline{n\text{ MOS}}$

$L = 1 \mu\text{m}$

$W = 1 \mu\text{m}$

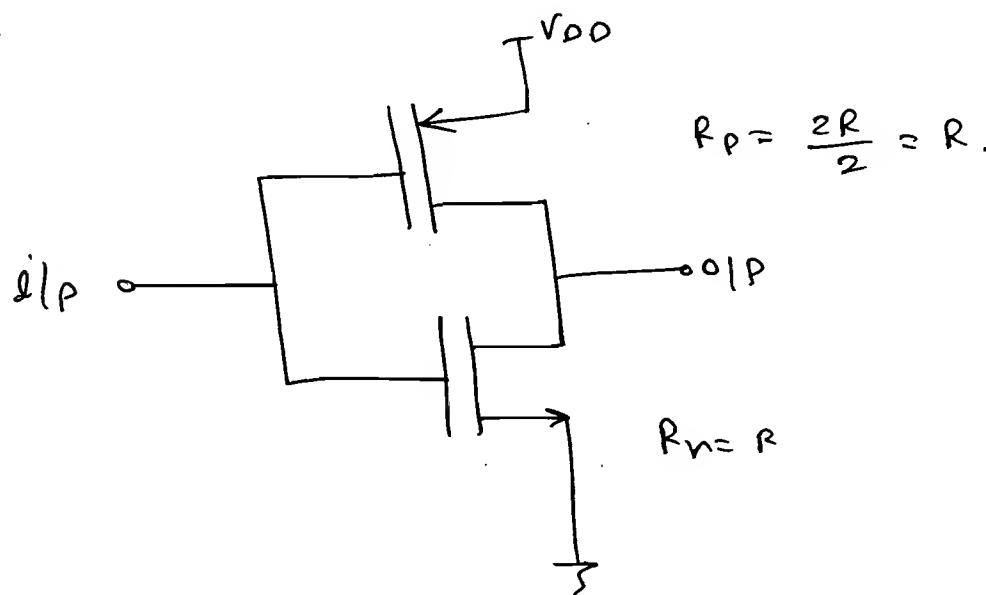
P MOS

$L = 1 \mu\text{m}$

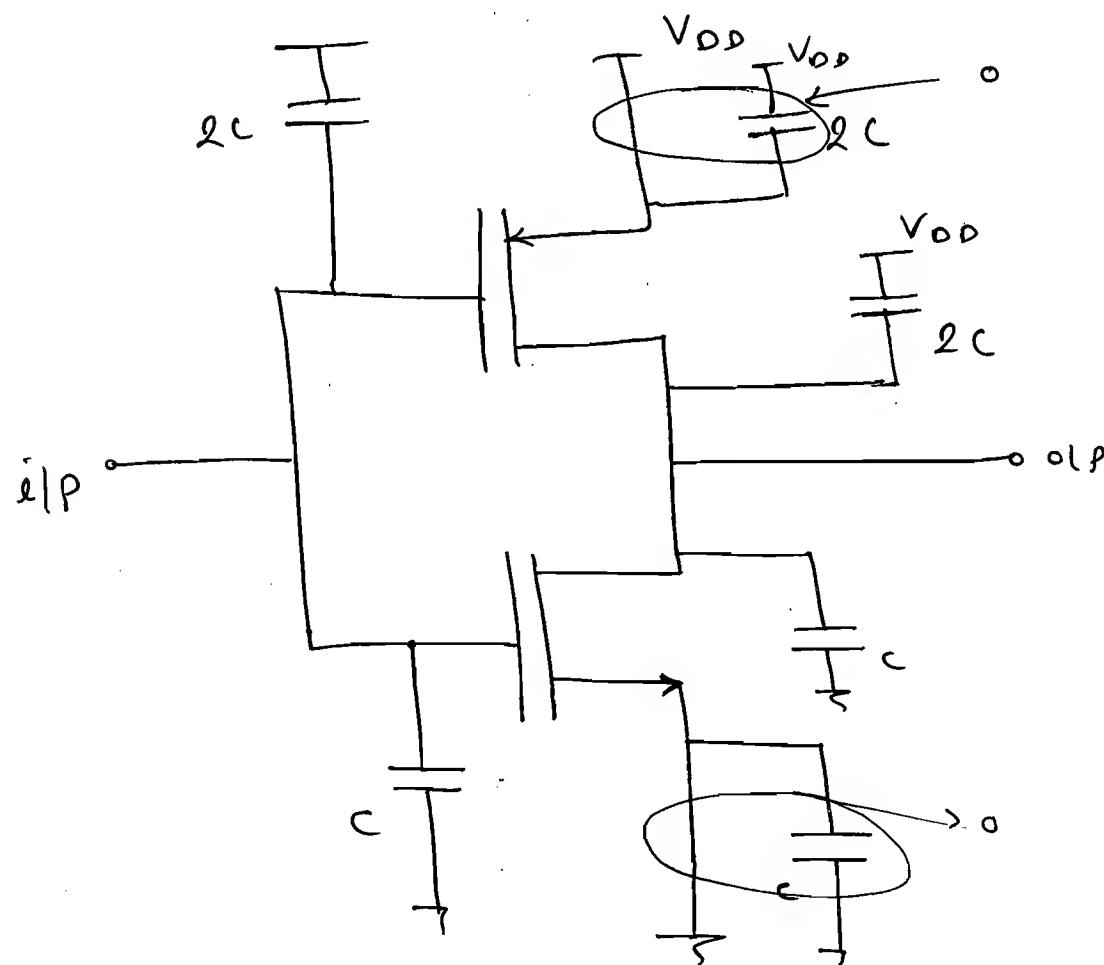
$W = 2 \mu\text{m}$

74)

*

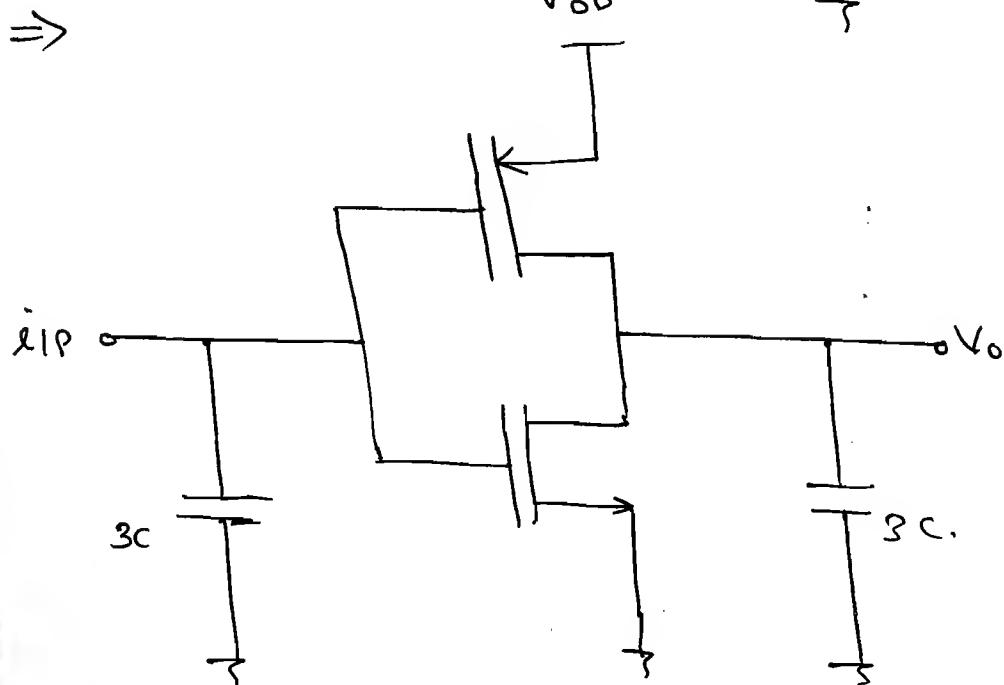
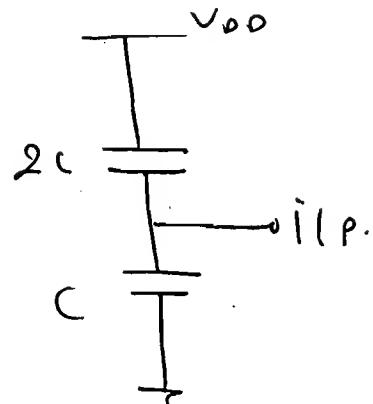


*



$$(C \propto \frac{\omega}{L})$$

\Rightarrow i/p capacitance,

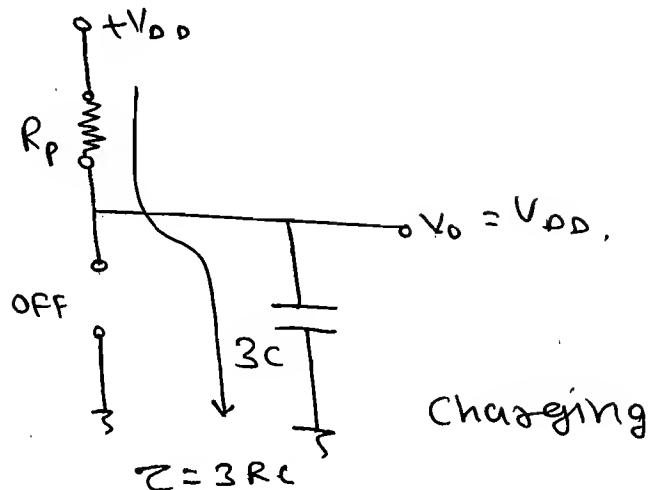


$$\Rightarrow ① V_i = 0$$

\Rightarrow NMOS : OFF

\Rightarrow PMOS : ON

$$\text{Rise time } (t_{\text{pdr}}) = 3CR_p.$$

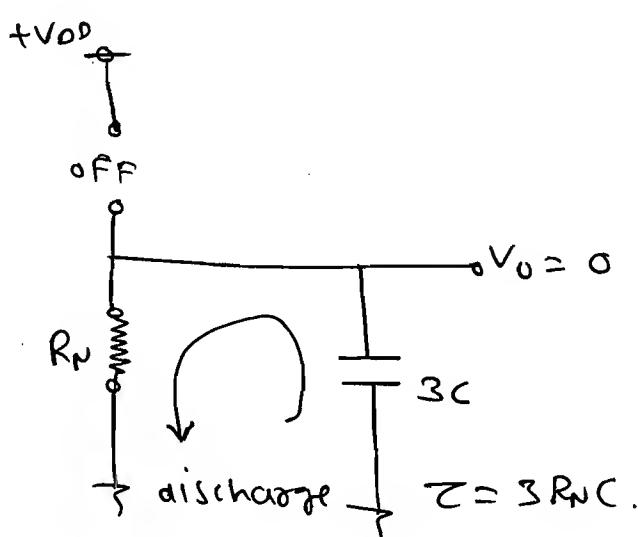


$$\Rightarrow ② V_i = V_{DD}.$$

\Rightarrow NMOS : ON.

\Rightarrow PMOS : OFF.

$$\text{Fall time } (t_{\text{paf}}) = 3R_n C.$$

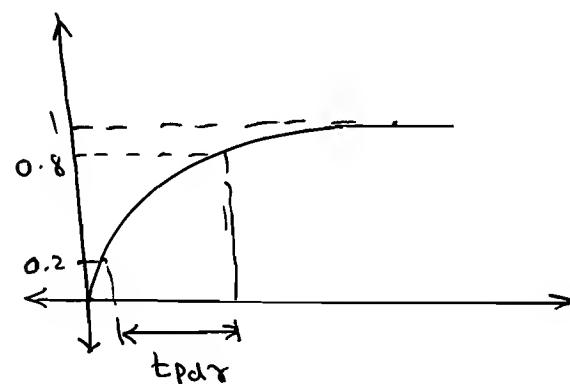


* Propagation Delay:

$$(t_{pd}) = \frac{t_{par} + t_{paf}}{2}$$

* Rise-time (t_{par}):

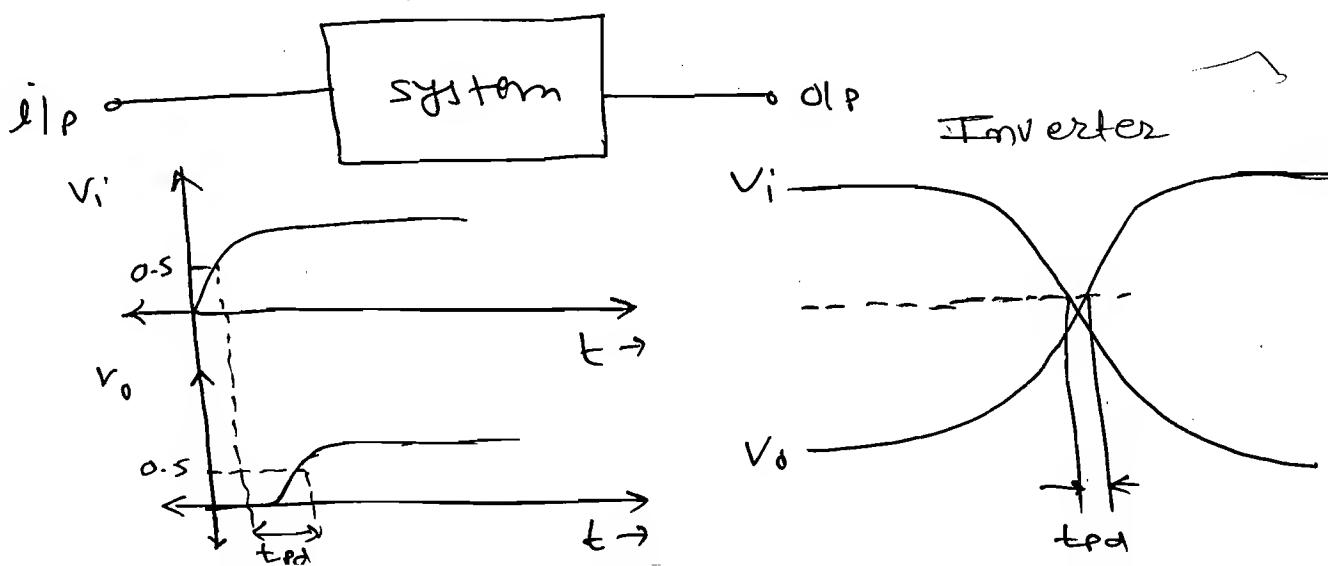
⇒ It is the time taken by the waveform to rise from 20% to 80% of its steady state value.



② Fall time (t_f):

⇒ It is the time taken by the waveform to fall from 80% to 20% of its steady state value.

③ Propagation delay (t_{pd}):



⇒ it is the max. time from the 0% crossing to the 0% crossing 50%.

④ Contamination Delay: (t_{cd}):

⇒ It is the minimum time from the input crossing 50% to the 0% crossing 50%.

★ Power Calculation:

1. Dynamic power 2. Static power.

① Dynamic power:

⇒ Dynamic power is the power consumed by the MOSFET during its transition. i.e. it is the power consumed by the MOSFET during switching (or) Transition from Logic '1' to Logic '0' (or) from Logic '0' to Logic '1'.

(i) Capacitor charging & discharging power.

(ii) Short ckt power & Conduction power.

(i) Capacitor charging & discharging power:

⇒ The energy dissipated across the ~~Extrinsic~~ P-mos transistor during capacitor charging,

$$E_c = \frac{1}{2} C \cdot V_{DD}^2$$

⇒ The energy dissipated across the nmos transistor during discharging

$$E_o = \frac{1}{2} C \cdot V_{DD}^2$$

⇒ Total energy dissipated across pmos & nmos Transistors = $E_o + E_c$

$$\therefore E = C V_{DD}^2$$

$$\therefore \text{Power } P = \frac{E}{T} = \frac{C V_{DD}^2}{T}$$

$$\therefore P = C V_{DD}^2 \cdot f$$

Time period
freq^{1/2} of switching

$$P_{\text{charge \& discharge}} = C V_{DD}^2 \cdot f$$

(ii) Short Ckt Power:

Req

Condⁿ

Pmos

Nmos

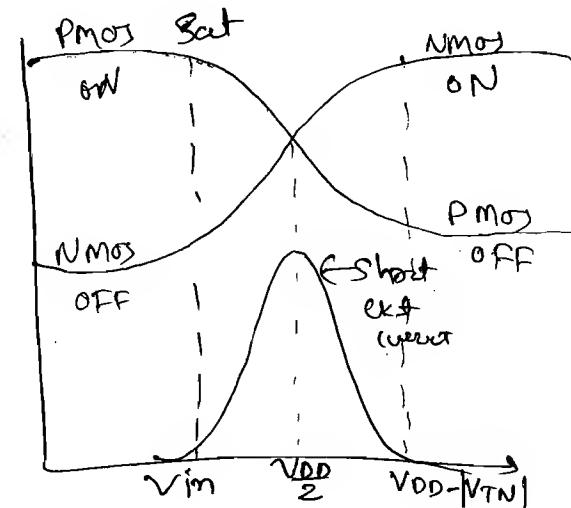
C

$$V_i = \frac{V_{DD}}{2}$$

Sat

Sat

P_{short}



⇒ Total Dynamic Power = $P_{\text{charge \& discharge}} + P_{\text{short ckt}}$

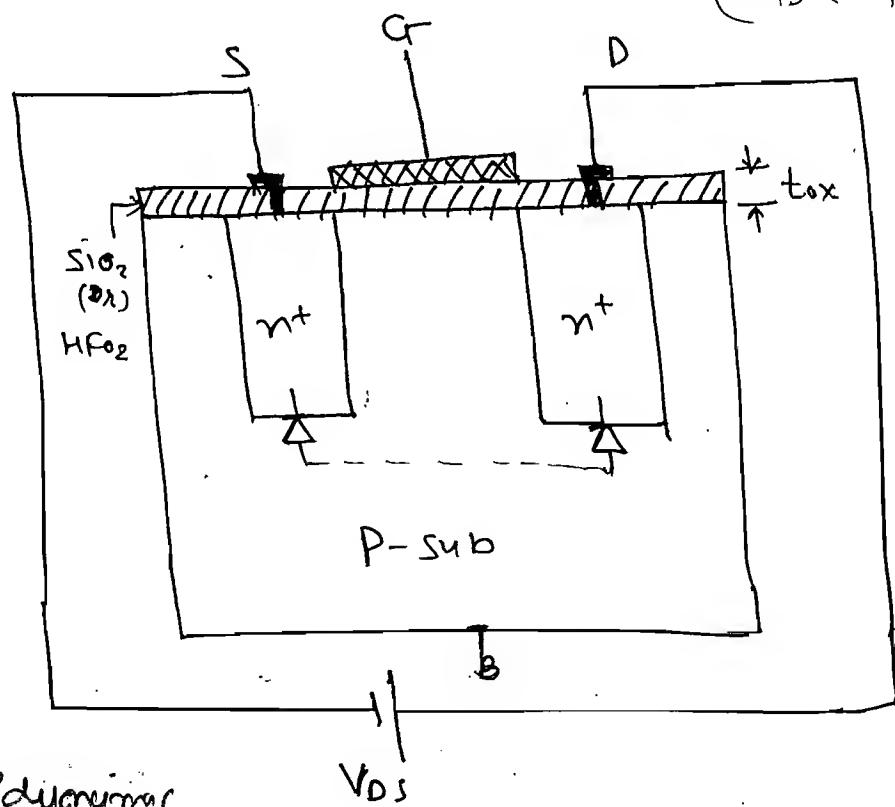
$$\approx P_{\text{charge \& discharge}}$$

$$\text{Dynamic} = C V_{DD}^2 \cdot f$$

(2.) Static Power:

⇒ Static power is the power consumed by the MOSFET during ideal state i.e. it is the power consumed by the MOSFET during Continuously ON at Logic '1' state (or) Continuously OFF Logic '0' state. & this is due to

- (i) Gate oxide leakage current. ($I_{g\text{leakage}}$).
- (ii) junction leakage current. ($I_{j\text{leakage}}$).
- (iii) Subthreshold leakage current. (I_{subleak}). ($V_{GS} < V_T$)



$$\epsilon_{SiO_2} = 3.9$$

$$\epsilon_{HfO_2} = 30.$$

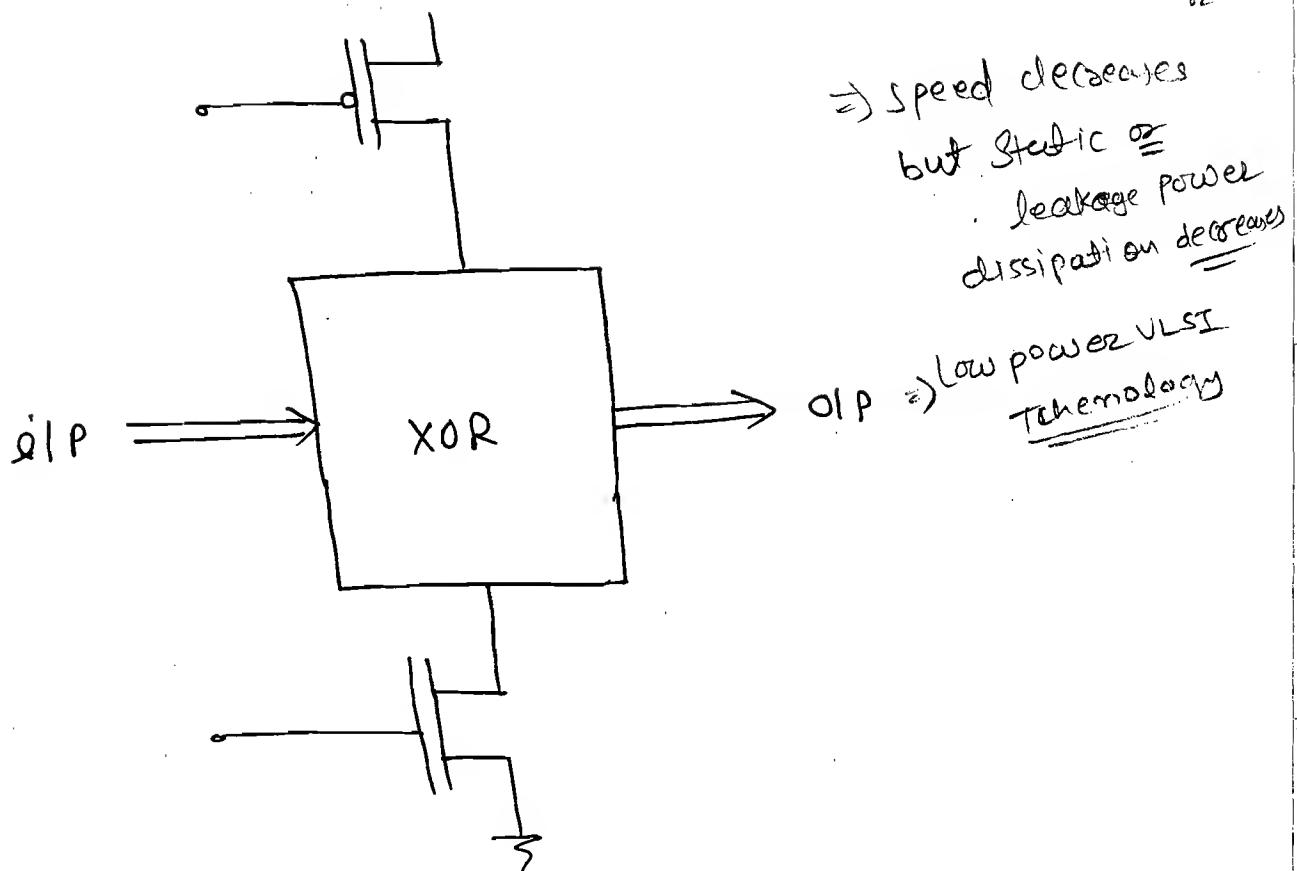
up to
90nm

Polym > P_{stat}
below 90nm

$P_{\text{static}} > \text{Polymeric}$

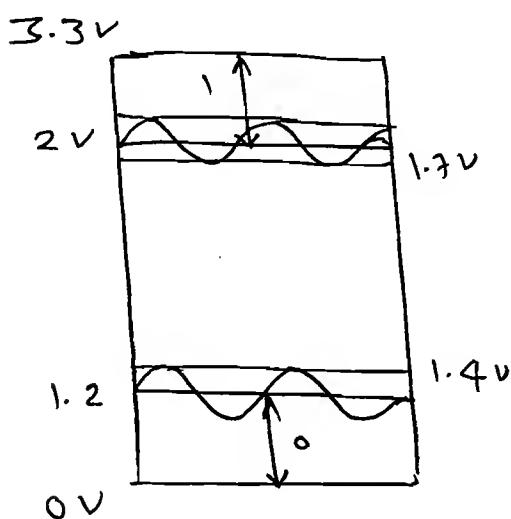
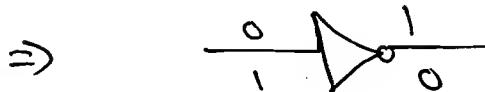
$$\Rightarrow P_{\text{static}} = (I_{g\text{leakage}} + I_{j\text{leakage}} + I_{\text{subleak}}) V_{DD}$$

$$\therefore P = P_{\text{dynamic}} + P_{\text{static}}.$$



* Noise Margin:

⇒ Noise Margin allows you to determine maximum allowable noise voltage at the input of the gate without disturbing output.

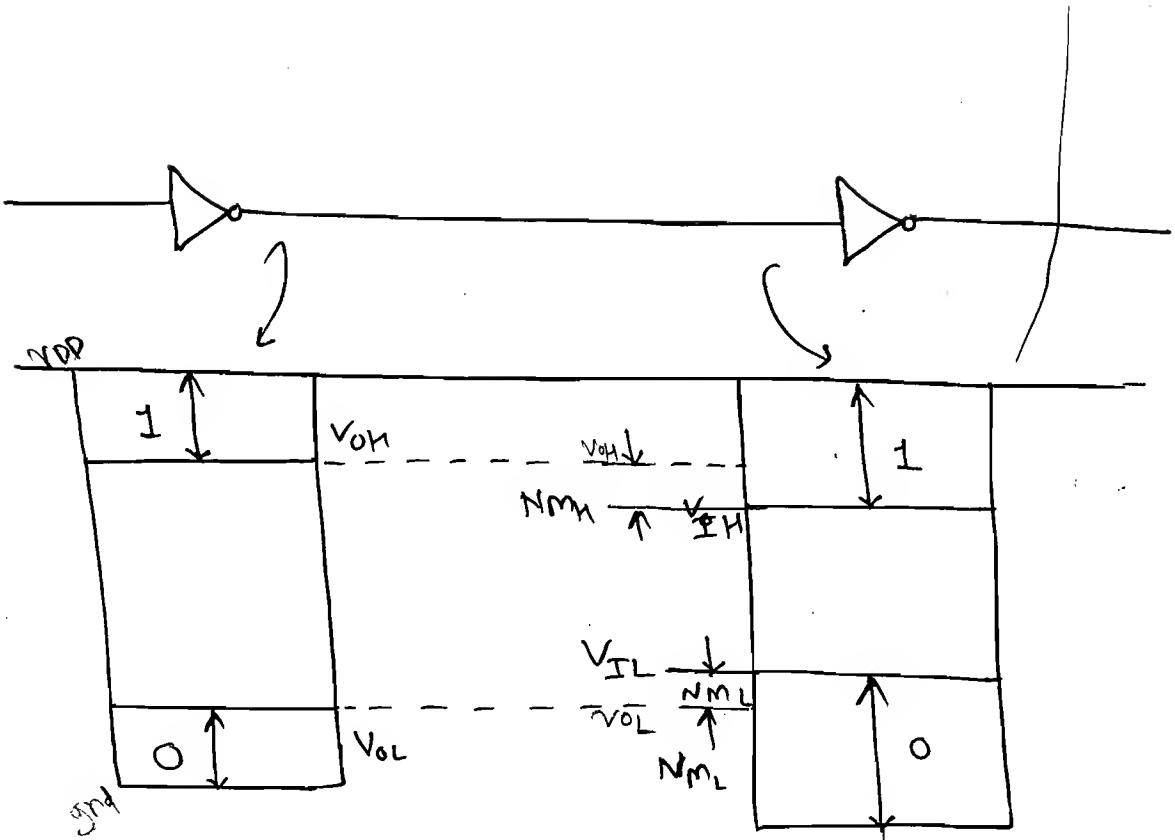


① High Noise Margin.
(NM_H):

$$NM_H = V_{OH} - V_{IH}$$

② Low Noise Margin.
(NM_L):

$$NM_L = V_{IL} - V_{OL}$$



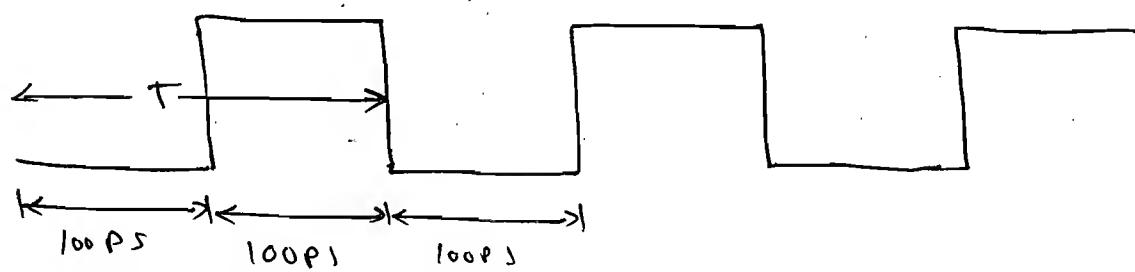
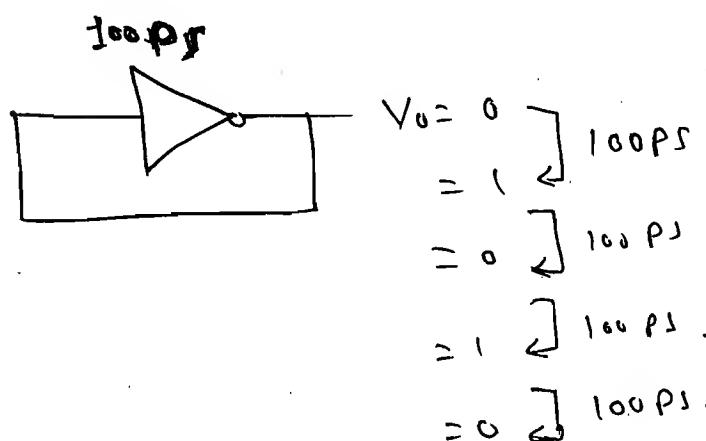
→ V_{th} : Dose. Min. High old voltage.

V_{IH} : ~~Max.~~ High Min. High IIP Voltage.

V_{OL} : Max. Low OIP Voltage.

V_{IL} = max. Low IIP voltage.

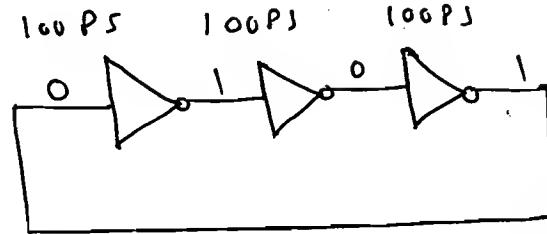
$$V_{OL} < V_{IL} < V_{IH} < V_{OH}.$$



$$T = 200 \text{ ps.}$$

$$f = \frac{1}{200 \text{ p}} \text{ Hz}$$

\Rightarrow



Ring oscillator

$$V_0 = 0 \Rightarrow 300 \text{ ps}$$

$$V_0 = 1 \Rightarrow 300 \text{ ps}$$

$$V_0 = 0 \Rightarrow 300 \text{ ps}$$

$$V_0 = 1 \Rightarrow 300 \text{ ps}$$

$$T = 600 \text{ ps}$$

$$f = \frac{1}{600 \text{ ps}}$$

$\Rightarrow N = \text{no. of inverters}$

$n = \text{delay of each inverter}$

inverter.

applicable only for
some time delay
for every inverter
& no. of inverters
is fixed

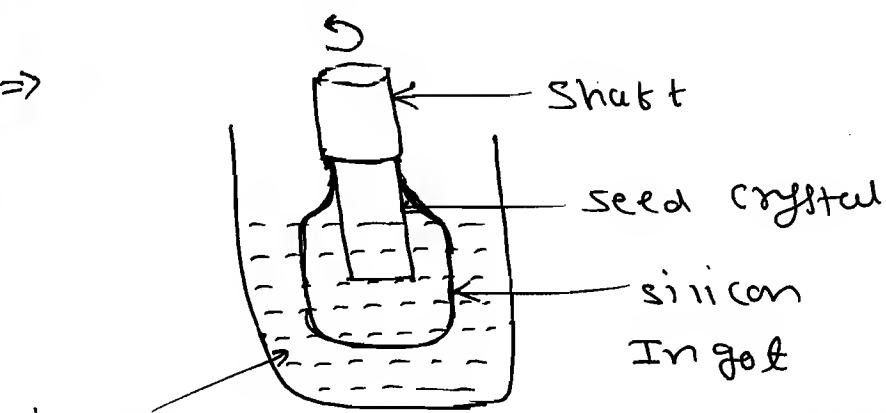
$$\therefore f_0 = \frac{1}{2 \times 3 \times 100} = \frac{1}{600 \text{ p}} \text{ Hz.}$$

★ Device Technology

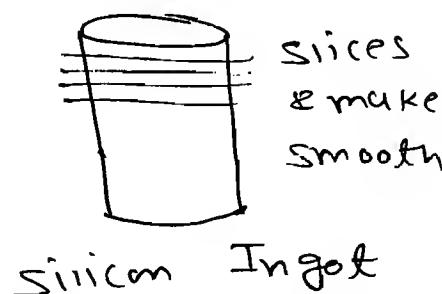
1. Crystal growth and wafer preparation.
2. Oxidation. $\xrightarrow{(2)}$ Epitaxy
3. Photolithography.
4. Diffusion.
5. Ion - Implantation.
6. Metallization.
7. Passivation.
8. Packing.

(1) Crystal growth $\xrightarrow{(3)}$ vacuum evaporation of aluminum and wafer prep.

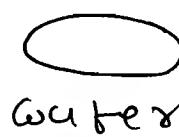
\Rightarrow Czochralski Process:



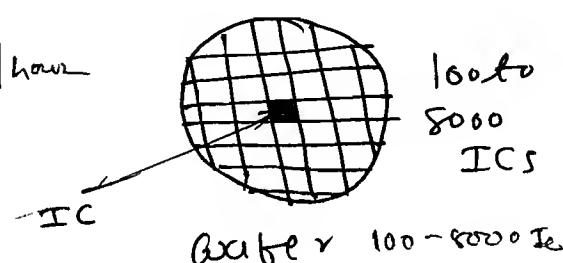
impurity 99.99999
 1425°C growth rate 30-180mm/hour
 $100\text{ cm} \rightarrow$ length
 $15\text{ cm} \rightarrow$ diameter



silicon Ingot



wafer

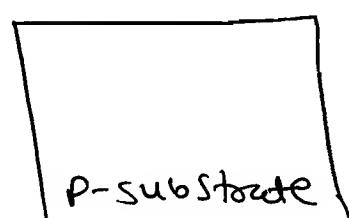


wafer 100-8000 μm

\Rightarrow wafer thickness = 16 to 32 mil.

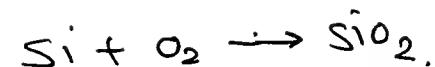
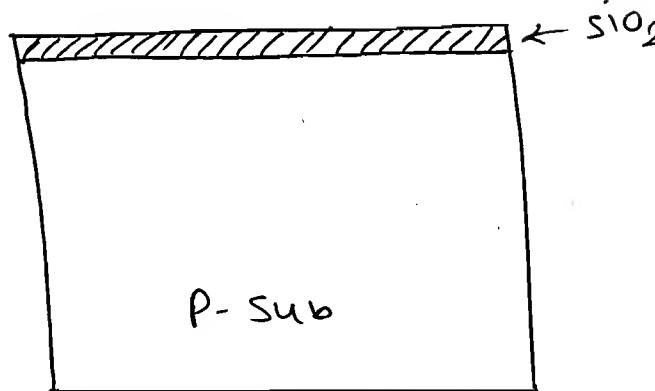
1 mil \approx 25 μm

\Rightarrow Diameter : 75 to 300mm.



p-substrate

(2) oxidation:



84

⇒ It is easy to form SiO_2 on top of the silicon without adding any extra material.

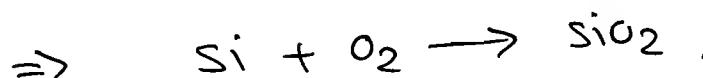
⇒ It doesn't allow any impurity through it.

⇒ It dissolves only in hydrochloric acid.

⇒ SiO_2 is a dielectric material; therefore it can be used as a ~~an~~ insulator (or) isolator bet'n two devices (or) two stages.

⇒ There are two methods of oxidation:

① Dry oxidation:



→ take place at $1200^{\circ}C$.

→ Slow process.

→ Thin layers.

→ Dry oxidation is a slow process. But

the electric properties of Dry oxidation
is better than wet oxidation.

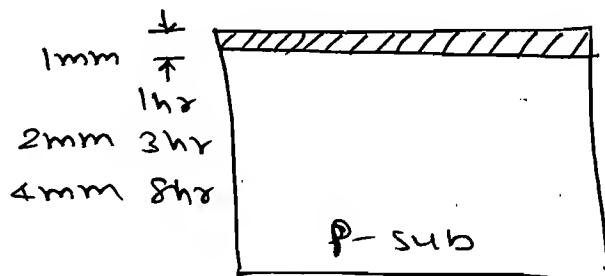
(ii) Wet oxidation:



\rightarrow 900° to 1000°C

\rightarrow Fast

\rightarrow thick layers.



(iii) Photolithography:

\Rightarrow Photo \rightarrow ~~picture~~ lights

Lithos \rightarrow Stone

Graphy \rightarrow picture.

\rightarrow (i) Photoresist ✓

(ii) Photo mask. ✓

(iii) UV rays. ✓

(iv) Developing. ✓

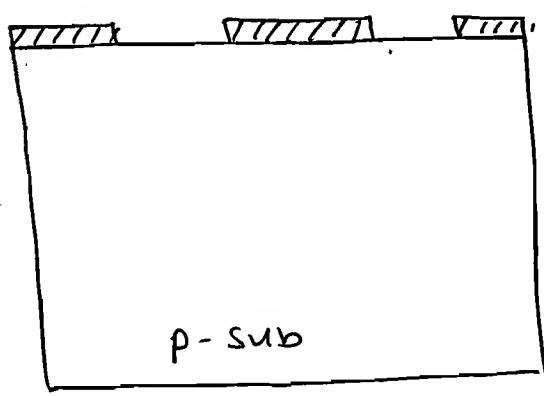
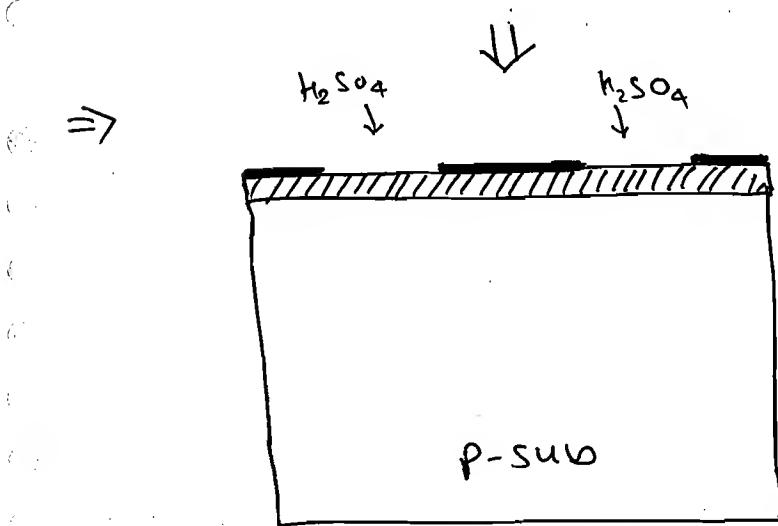
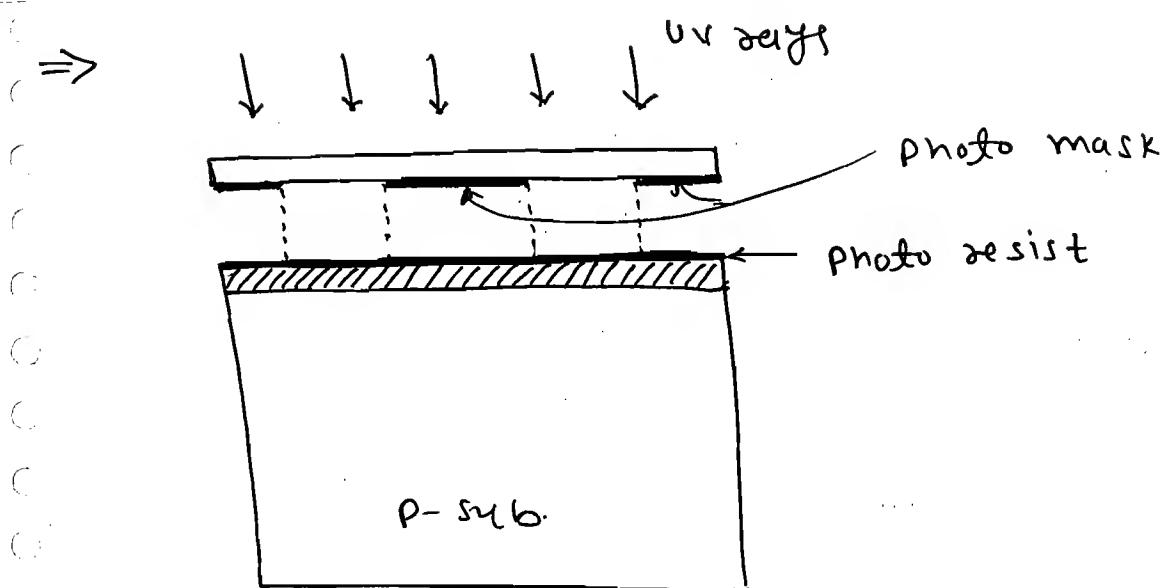
(v) Etching..

(vi) Stripping..

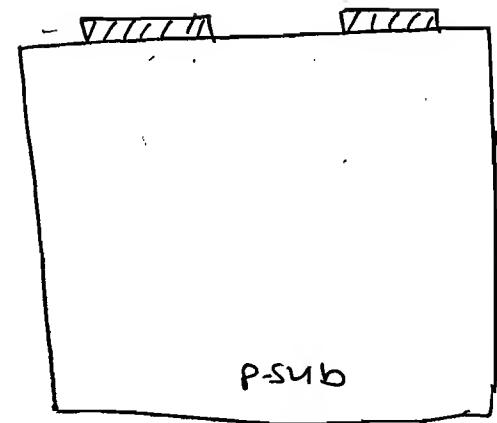
\Rightarrow Stripping is a process of removing unwanted portion.

\Rightarrow Photo resist:

- ① Positive photo resist
- ② Negative photo resist.



positive photo resist

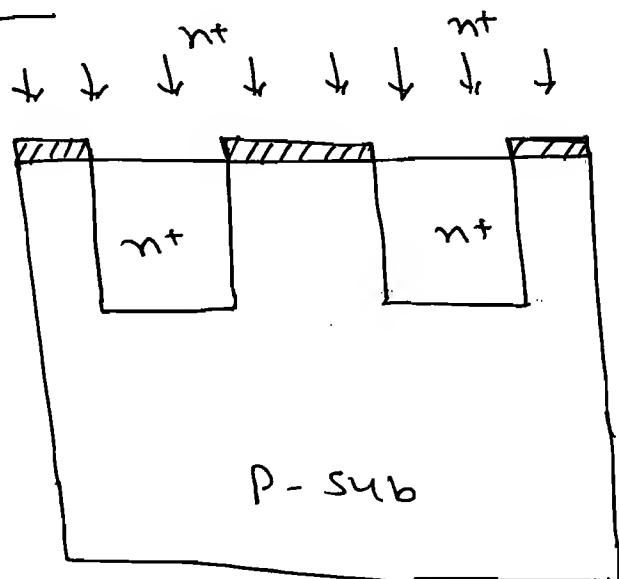


negative photo resist.

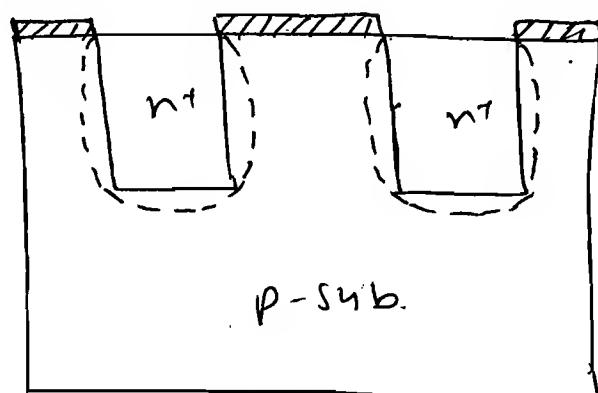
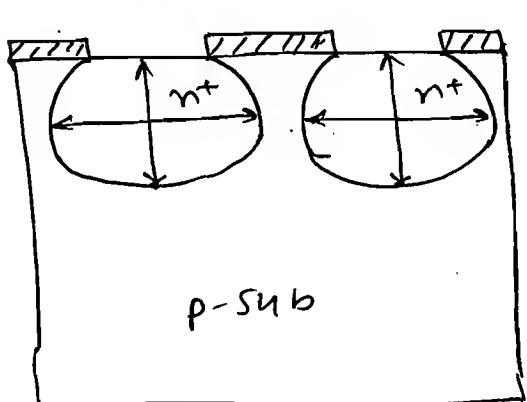
⇒ The portion of the silicon dioxide which is exposed to uv rays if it gets removed during etching process then it is called positive photo resist.

⇒ The portion of the silicon dioxide which is not exposed to UV rays if it gets removed during etching then it is called -ve photo resist.

(4) Diffusion:



(i) Isotropic diffusion: (ii) Anisotropic diffusion:



⇒ Take Place: 1000°C

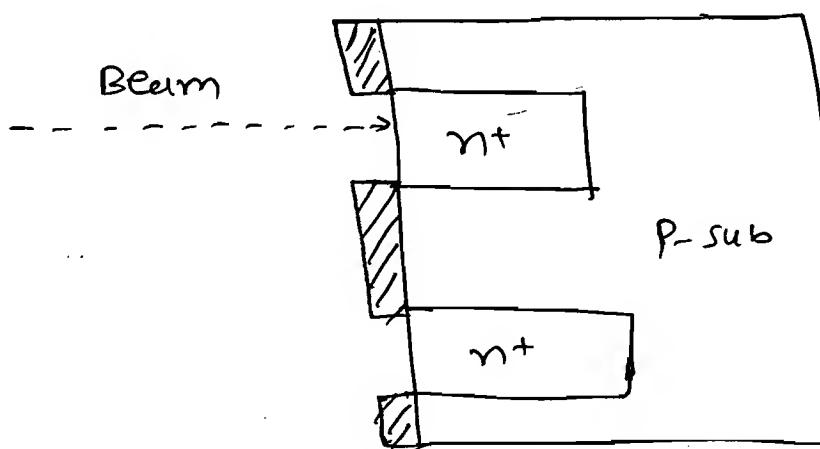
⇒ for n+ type: P_2O_5 , $POCl_3$ (Phosphorus oxide)

⇒ for p+ type: B_2O_3 , BCl_3 .
(S & O)

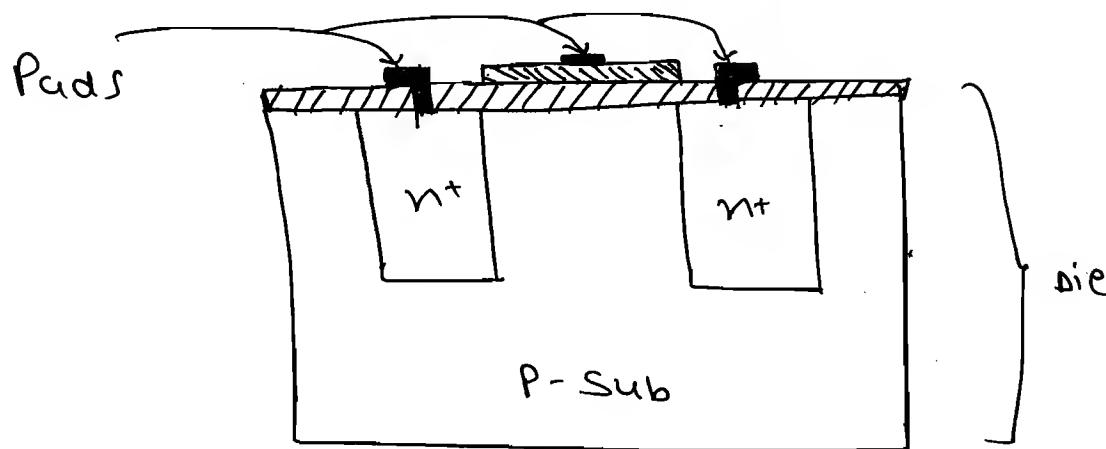
(5) Ion - Implementation:

⇒ It is also same as diffusion process but it take place at lower temperature and slow process.

⇒



(6) Metalization:



⇒ Metalization is a process of forming metallic contact betⁿ the device for inter connection.

⇒ Old design: Al

⇒ New design: Cu

$(\sigma_{Cu} > \sigma_{Al}) \Rightarrow$ to reduce Contact resistance.

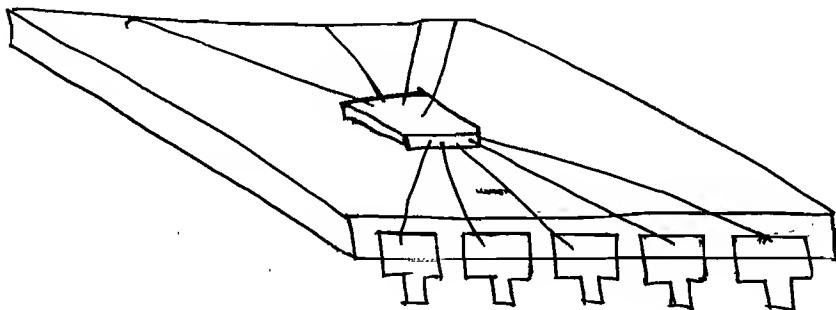
(7.) Passivation:

⇒ Passivation is a process of forming glass type of epoxy coating on the surface of the die to protect it from the atmosphere and also to provide mechanical strength.

(8) Packing:

Die: 10 to 207.

⇒



- more than 200 types of packing.
- DIP package.
- PLCC, QFN
- PGFA (pin grid array).
- BGA (Ball grid array)

↑
Low Power like memories, MP.

